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SUMMARY OF SIGNAL PROCESSING TECHNIQUES FOR CONFORMAL/PLANAR AR--ETC(U)
MAR 66 M T STARK NOBSR-93022
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Technical Memo

Summary of Signal Processing Techniques for Conformal/Planar Array Sonar System (U)

7 March 1966

Contract NObsr 93022
Project Serial Number SS-048-00
Task 8189
(GE Requisition Number EH-88157)

Prepared by

General Electric Company
Heavy Military Electronics Division
Syracuse, N.Y.
Electronics Sys.

Prepared for

Navy Department Bureau of Ships
U.S. Navy Electronics Laboratory
San Diego, California

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for

Conformal/Planar Array Sonar System (U)

CONFORMAL/PLANAR ARRAY SONAR PROJECT

March 1966

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SECTION I

INTRODUCTION

This report covers work done on signal processing technique studies during the period from January 1, 1966 to February 28, 1966 on the Conformal/Planar Array Sonar Contract NObsr 93022.

A previous report entitled "The First Cut Signal Processor for Conformal/Planar Array Sonar System", (1) in which a feasible signal processing sub-system for the C/PAS System was recommended, contains much of the background material for the work reported here. In the course of this work various techniques were studied under the requirements imposed by the C/PAS System concept, ~~as outlined in references 2 and 3.~~ Since the system concept presented in these references may be quite different from the system concept that is finally chosen, it was deemed appropriate to review the technique studies that were previously made and to determine their range of applicibility in terms of signal bandwidth and number of beams to be processed.

Therefore, the purpose of the work reported here is to:

(1) Review the technique studies previously conducted to determine feasibility of these techniques for various combinations of signal bandwidth and number of beams. Specifically, bandwidths in the range of 50 to 200 cps for the wide-band signals, 1 to 4 cps for the narrow band signal, and number of beams in the range of 100 to 1000 were assumed.

(2) Extend the studies previously conducted to include cost and size estimates for hardware implementations of the First Cut Signal Processing Sub-System, as well as for other techniques studied, as a function of signal bandwidth and number of beams.

(3) Identify critical components of the most promising techniques which require further detailed study and/or laboratory breadboard work in order to raise confidence level for application to the C/PAS System.

Section II contains a summary of the important features of the signal processing techniques which have been studied to date as well as a table showing requirements under which the studies were made.

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Section III summarizes the results of the studies of cost as a function of signal bandwidth and number of beams.

In Section IV critical parts of promising techniques are identified and recommendations for further study are given.

Sections V, VI and VII contain the details of the cost studies for the surface duct, narrowband bottom bounce, and wideband bottom bounce techniques.

SECTION II

SUMMARY OF TECHNIQUE STUDIES

The purpose here is to summarize signal processing requirements as well as the important features of signal processing techniques that have been studied to date and to outline requirements and techniques for future study.

The requirements for technique studies are given in Table 2. In this table requirements 1, 2, 3 and 5 are the same as the requirements under which previous techniques were studied. A more detailed description of these requirements is to be found in the First Cut Signal Processor Report.(1) It is proposed that future signal processing techniques be studied under requirements 1, 2, 4, 5 and 6. This set of requirements differs from the first set in two ways. First, requirement 4 is substituted for requirement 3. These two requirements differ only in the variable pulse length part. Requirement 3 specifies that the processor have two switching functions, one switch having the capability of selecting the number of beams to be processed and the other having the capability of selecting one of a number of processor configurations which are designed to handle different pulse lengths. Under requirement 4 these two switching functions are eliminated. Therefore, each signal processing configuration studied under this requirement will only have the capability of processing a given number of beams and a particular signal. The reason for changing this requirement is that the particular combinations of number of beams and pulse lengths that should be designed into the signal processor should be chosen to be consistent with the C/PAS System Concept. Inputs from system studies are needed before these combinations can be selected. Until the time when such inputs are available, signal processing studies will be conducted under requirement 3 but keeping in mind that a requirement similar to requirement 4 may eventually be imposed.

Requirement 4 and 6 are nearly the same except for the application and the fact that the wideband processor is required to process only zero doppler targets while the surface duct processor is required to process targets in the doppler range ± 50 cps.

Table 1 illustrates the categories under which technique studies conducted to date and future technique studies will be summarized. Even though a tentative selection of the techniques listed in this table has been made for the First Cut Signal Processor, all of the techniques listed are still considered to be candidates for the Experimental Ship System. The cascaded VICI technique which is described in detail in reference 4 has been eliminated from further consideration because of the large number of delay lines required and the cost relative to the VICI technique which is described in the First Cut Signal Processing Report. The dispersive network or delay line technique was considered for processing a linear FM pulse and has been eliminated from further consideration because of the difficulty of physically realizing large values of dispersion over a relatively small bandwidth. The requirements are prohibitive even for a signal bandwidth of 100 cps and a BT = 5. The requirement is increasingly severe with increase in signal BT product.

Further details of all of the signal processing techniques in Table 2 are given in the appropriate references at the end of this report.

During the period from March to June 1966, the study of signal processing techniques will continue. The techniques which will be studied are discussed in the paragraphs that follow.

N-Bit Correlator - This type of correlator will be studied for the wideband bottom bounce and the surface duct applications. The technique differs from the clipped correlator processor in the following ways: (1) The limiter is replaced by an A/D converter, (2) The time compressed digital words are D/A converted in order to achieve an analog correlation, (3) The storage requirements and the processor dynamic range both increase with increase in the number of bits, (4) The advantage of normalization obtained by hard limiting is lost.

TIMAC - This correlator will be studied for the wideband bottom bounce and surface duct applications. This is a one bit coding scheme that uses delta modulation in place of the polarity sampling done in the clipper correlator. Except for the method of coding it is substantially similar to a clipped correlator. The dynamic range of the device is related to the number of samples used in the correlation

and the feedback characteristic used in the encoding. This technique appears to have the capability of accomplishing the equivalent of a multibit correlation with a concurrent saving in storage capacity.

Reference Clipped Hetroline Correlator - This technique will be studied for the wideband bottom bounce and surface duct applications. The concept here is that the reference signal be limited and the polarity samples stored in a recirculating memory without time compression. The clipped reference is used to correlate with the received analog signal. The reference storage requirements are considerably reduced in comparison to an analog correlator, but real time operation may still require a prohibitive amount of hardware.

Analog Tapped Delay Line Processors - For both the wideband bottom bounce and surface duct modes, tapped delay line processors are likely candidates for a variety of waveforms. It appears that magnetostructive delay lines probably up to 100 milliseconds are feasible, with reservations concerning dynamic range, spurious, and bandwidth limitations on this type of delay line.

Other digital processors - To date a single digital processing technique was studied for the narrowband bottom bounce mode. It is intended here to study other digital techniques for this mode of operation as well as studying techniques for the wideband bottom bounce and surfact duct modes.

1.	Technique	Simple Pulse Processor BT = 1 T = 10 ms B = 100 cps
2.	Requirement and Application	table #2 2,5 - WBBB & SD
3.	Input Signal Format	N Inputs on N Wires
4.	Output Signal Format	Time Multiplexed, Analog, Detected
5.	Sample Rate Per Beam	400 cps
6.	Storage Requirement	None
7.	Dynamic Range	60 db
8.	Cost (225 beams)	175K
9.	Cabinets (225 beams)	1 1/2
10.	Critical Components	High dynamic range detector
11.	Stage of Development	Can be built with transistors
12.	Coh/Noncoherent Flexibility	Switch post detection filters
13.	Feasibility	Feasible with high confidence (except detector)
14.	Advantages	Simple, reliable, high dynamic range, direct display capability
15.	Disadvantages	Cost and Size

TABLE 1

SUMMARY OF TECHNIQUE FEASIBILITY STUDY

1.	Technique	VICI BT = 1, T = 1/2 sec, B = 2 cps
2.	Requirement & Application	1, NBBB
3.	Input Signal Format	Time multiplexed beams (analog)
4.	Output Signal Format	Time sequence of doppler bins for each beam in sequence (analog)
5.	Sample Rate/Beam	136 cps
6.	Storage Requirement	Two 3676 μsec Quartz delay lines
7.	Dynamic Range	60 db
8.	Cost (225 beams)	25K
9.	Cabinets (225 beams)	1/4
10.	Critical Components	None
11.	Stage of Development	Applicable transistor hardware experience
12.	Coh/Noncoherent Flexibility	Not easily adaptable (needs further study)
13.	Feasibility	Feasible with high confidence
14.	Advantages	Cost, size, established technique
15.	Disadvantages	High output bandwidth

TABLE 1 (CONT.)

SUMMARY OF TECHNIQUE FEASIBILITY STUDY

1.	Technique	Digital Doppler Processor BT = 1, T = 1/2 sec, B = 2 cps
2.	Requirement & Application	1, NBBB
3.	Input Signal Format	Time multiplexed beams (analog)
4.	Output Signal Format	Time sequence of doppler bins for each beam in sequence (digital)
5.	Sample Rate/Beam	I & Q channels 100 cps per channel
6.	Storage Requirement	271,000 bit magnetic core memory or 24 - 10 ms delay lines
7.	Dynamic Range	36 db (6 bit encoder)
8.	Cost (225 beams)	35K
9.	Cabinets (225 beams)	1/2
10.	Critical components	None
11.	Stage of Development	No hardware - concept verified by digital simulation.
12.	Coh/Noncoherent flexibility	Provisions are easily made
13.	Feasibility	Feasible - commerciably available components for required data rates.
14.	Advantages	Digital output, design flexibility, eventual implementation in micro-circuits
15.	Disadvantages	Cost & size, range and doppler splitting losses

TABLE 1 (CONT.)

SUMMARY OF TECHNIQUES FEASIBILITY STUDY

1.	Technique	Clipper correlator BT = 8, T = 80 ms, B = 100 cps
2.	Requirement & Application	2,5 WBBB and SD
3.	Input Signal Format	Time multiplexed clipped beam inputs
4.	Output Signal Format	Time sequence of correlation values for each beam in sequence
5.	Sample Rate/Beam	200 cps
6.	Storage Requirement	Two 500 μsec delay lines one 120 stage shift register
7.	Dynamic Range	
8.	Cost (225 beams)	15K
9.	Cabinets (225 beams)	1/4
10.	Critical Components	None
11.	Stage of Development	Applicable experience with SQS-26 correlator
12.	Coh/Noncoherent Flexibility	
13.	Feasibility	Feasible with high confidence
14.	Advantages	Cost & Size - normalized output, flexible with regard to signal coding
15.	Disadvantages	Distortion due to limiting, output format requires demultiplexing

TABLE 1 (CONT)

SUMMARY OF TECHNIQUE FEASIBILITY STUDY

1.	Technique	Scanned Filter BT = 1, T = 1/2, B = 2 cps
2.	Requirement & Application	1, NBBB
3.	Input Signal Format	Time multiplexed beams (analog)
4.	Output Signal Format	Time sequence of doppler bins for each beam in sequence (analog)
5.	Sample Rate/Beam	300 cps
6.	Storage Requirement	589,824 bit magnetic core memory
7.	Dynamic Range	48 db (8 bit encoder)
8.	Cost (225 beams)	125K
9.	Cabinets (225 beams)	2 1/2
10.	Critical Components	D/A Converter (8 bit, 7.66 Mc)
11.	Stage of Development	Applicable transistor hardware experience
12.	Coh/Noncoherent Flexibility	Switch predection filter
13.	Feasibility	Feasible with high confidence (D/A converter is a development item)
14.	Advantages	Easily adopted to shorter pulses, High dynamic range, Flexible memory
15.	Disadvantages	Requires A/D & D/A converters. cost and size · range & frequency splitting losses.

TABLE 1 (CONT.)

SUMMARY OF TECHNIQUE FEASIBILITY STUDY

TABLE 2

REQUIREMENT FOR C/PASS SIGNAL PROCESSING TECHNIQUE STUDIES

Requirement Number	Application	# Beams	Type of Pulse	Pulse Length (T)	Band-Width (B)	BT Product	Doppler Freq. Range	# Doppler Bins	Dynamic* Range	Comments
1	Narrow Band Bottom Bounce	225 Nominal 100-1000	CW	1/2 sec nom 1/4 to 1 sec	$\frac{1}{T}$	1	100 cps	50	48-60 db	Same as 1st cut
2	Wide Band Bottom Bounce	225 Nominal 100-1000	CW	10 ms 5-100 ms	$\frac{1}{T}$	1	$\frac{1}{T}$	1	48-60 db	Same as 1st cut
3.	Wide Band Bottom Bounce	225 100-1000	LFM	Variable	100 cps	Variable	100 cps	1		Same as 1st cut
4.	Wide Band Bottom Bounce	225 100-1000	LFM or Quadratic Phase Code	100 ms 10 ms - 1/2 sec	100 cps 50-200 cps	5-50**	B	1	48-60 db	
5.	Surface Duct	200 100-1000	CW	10 ms 5-100 ms	$\frac{1}{T}$	1	100 cps	No. Doppler Processing	48-60db	Same as 1st cut
6.	Surface Duct	200 100-1000	LFM or Quadratic Phase Code	100 ms 10 ms- 1/2 sec	100 cps 50-200 cps	5-50**	100 cps		48-60 db	

NOTES: * A dynamic range goal in the 48-60 db range appears desirable. However, techniques with lower dynamic range should not be omitted from consideration on the basis of dynamic range alone.

** This Requirement restricts the range of combinations of B and T

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SECTION III

SUMMARY OF CRITICAL COMPONENTS

As a result of the technique studies to date, a number of the more important critical components that might be required in the final C/PASS signal processing equipment have been identified. For the most part specifications on these parts are such that near state-of-the-art design techniques or hardware are required for their implementation. As such, more detailed study and/or laboratory breadboarding is required to increase confidence in feasibility.

A brief description of each of the critical components is given below, with recommendations for further work.

The Adaptive Reverberation Filter - As described in the First Cut Signal Processing report, this filter is a relatively sophisticated part of the Narrowband Bottom Bounce Processor. It presently appears desirable that this notch be capable of automatically adjusting its notch depth and center frequency as a function of reverberation amplitude and center frequency. In the present signal processing concept one reverberation notch is required in each beam channel. Cost and size estimates reveal that this single item is a major contribution to both the cost and size of the Narrowband Bottom Bounce Processor. In addition, it is felt that realistic performance predictions of such a filter can best be obtained using sea tapes and either a laboratory breadboard or a digital simulation of the filter. It is therefore recommended that a design study of this filter be initiated, and that a breadboard model using microminiature circuits wherever possible be constructed and tested in the laboratory.

High Dynamic Range Envelope Detector - A 60 db dynamic range design goal was established for the simple pulse processors to be used in both the Surface Duct and Wideband Bottom Bounce Modes. This requirement does not appear to be critical for any of the components except the envelope detector. Such a dynamic range even for the relatively narrow 100 cps signal bandwidth is near state-of-the-art. Since such a detector is needed for every beam in both wideband and surface duct modes it is not only desirable to obtain the best possible performance, but the

design must be such that size, cost and power concumption are minimized. It is therefore recommended that laboratory work on improving the state-of-the-art of such a detector be continued.

Auto Gate High Power Amplifier - The preamplifier - delay line - post amplifier circuitry in the autogate for both the VICI and Scanned Filter processors will ultimately limit the dynamic range capability of this device. A 60 db dynamic range design goal on this device represents a near state-of-the-art or beyond state-of-the-art requirement for the VICI application. The requirement is perhaps more easily met for the scanned filter application since the bandwidth is somewhat lower. The dynamic range that can be achieved in this device is directly related to how hard the preamplifier can drive the delay line. It is estimated that to insure a 60 db dynamic range it is necessary that the preamplifier be designed to produce 70 volts into a 500Ω load over a 3 Mc video bandwidth. It is recommended that the required amplifier be designed, built, and tested.

D/A Converter for the Scanned Filter - The D/A converter for the Scanned Filter Processor described in the First Cut Signal Processing Report is required to make an 8 bit conversion at a 6.75 Mc rate. This represents a near state-of-the-art requirement and is the most critical component in the scanned filter processor. A D/A converter for a similar processor is presently being developed in house for the Naval Research Laboratory under Contract Nonr 4903-(00)X. The design goal for this D/A converter is to convert a 10 bit digital word at a 5 Mc rate. A paper design for this converter which utilizes integrated circuitry for the timing functions is completed and parts are on order. The present schedule calls for a completed product by August 1966. It is our intention to keep abreast of the progress on this development.

SECTION IV

SUMMARY OF COST STUDIES

The cost study was conducted in order to show how the cost and size of processors described in The First Cut Signal Processing report[1] vary as a function of the number of beams to be processed, signal bandwidth, and signal BT product. The study serves several important functions. It establishes the order of magnitude of the signal processing problem for the C/PASS application and shows the important contributors to size and cost within the signal processing subsystem itself. Furthermore, cost and size versus number of beams and signal bandwidth provides an important input to system cost effectiveness trade-off studies.

Estimates of numbers of circuit boards, filters, power supplies and other components were made in order to calculate cost and number of cabinets required. The cost figures and number of cabinets were calculated on the basis of "good commercial practice" utilizing transistor design techniques. Very little consideration was given to integrated or microminiature circuits. The costs are for materials only, and do not include costs for development and design or for system testing.

The general procedure for cost estimating was to first examine each of the blocks of a functional block diagram in order to decide the make or buy question. Outside vendor items were costed using previous quotes on similar items as well as catalogue information. For those items which would be built in house, the functional blocks were broken down to 2" x 4" circuit board level. An estimate of the number of such circuit boards for each function was then made. It was assumed that the cost for parts plus the time required to assemble and test an average 2" x 4" circuit board would be $100.

The sketch in Figure 1 illustrates a typical cabinet layout. The cabinet described has a frame 24" wide by 24" deep by 72" high. It has three drawers which contain the 2" x 4" circuit boards, power supplies and a blower. For the circuits built in house a packing density of 1500 2" x 4" circuit boards was assumed. Volume occupied by outside vendor items such as delay lines and magnetic core memories was estimated from previous quotes on similar items and catalogue information.

The ranges of variation selected for number of beams & signal bandwidth are as shown below:

Processor	Number of Beams	Signal Bandwidth
Narrowband processor	100 to 1000	1 cps to 4 cps
Wideband processor	100 to 1000	50 cps to 200 cps
Surface Duct Processor	100 to 1000	50 cps to 200 cps

It is assumed that within the range of variations shown that the component cost does not change as a function of the number of identical components required.

Since both the number of components and the cost per component can only be approximated at this time, the total cost and size figures are at best order of magnitude estimates. However, the relative cost and size as a function of signal bandwidth and number of beams should be more accurate.

Table 3 summarizes signal processor subsystem cost. The center column in this table represents cost for the First Cut Signal Processor for a narrowband bottom bounce pulse width of 1/2 sec, and wideband bottom bounce and surface duct signal bandwidth equal to 100 cps. The column on the left represents similar processor cost except that the narrowband pulse width is 1/4 sec, and the wideband and surface duct bandwidth is 50 cps. The third column is for a narrowband pulse width of 1 sec, and wideband and surface duct bandwidth of 200 cps. As shown in this table the total signal processor cost does not vary appreciably for change in signal parameters.

The table also serves to show that the predominant costs are in the narrowband preprocessor and the simple pulse processor.

Figure 2 shows the First Cut Signal Processor costs as a function of number of beams, all other parameters of the First Cut Processor being constant.

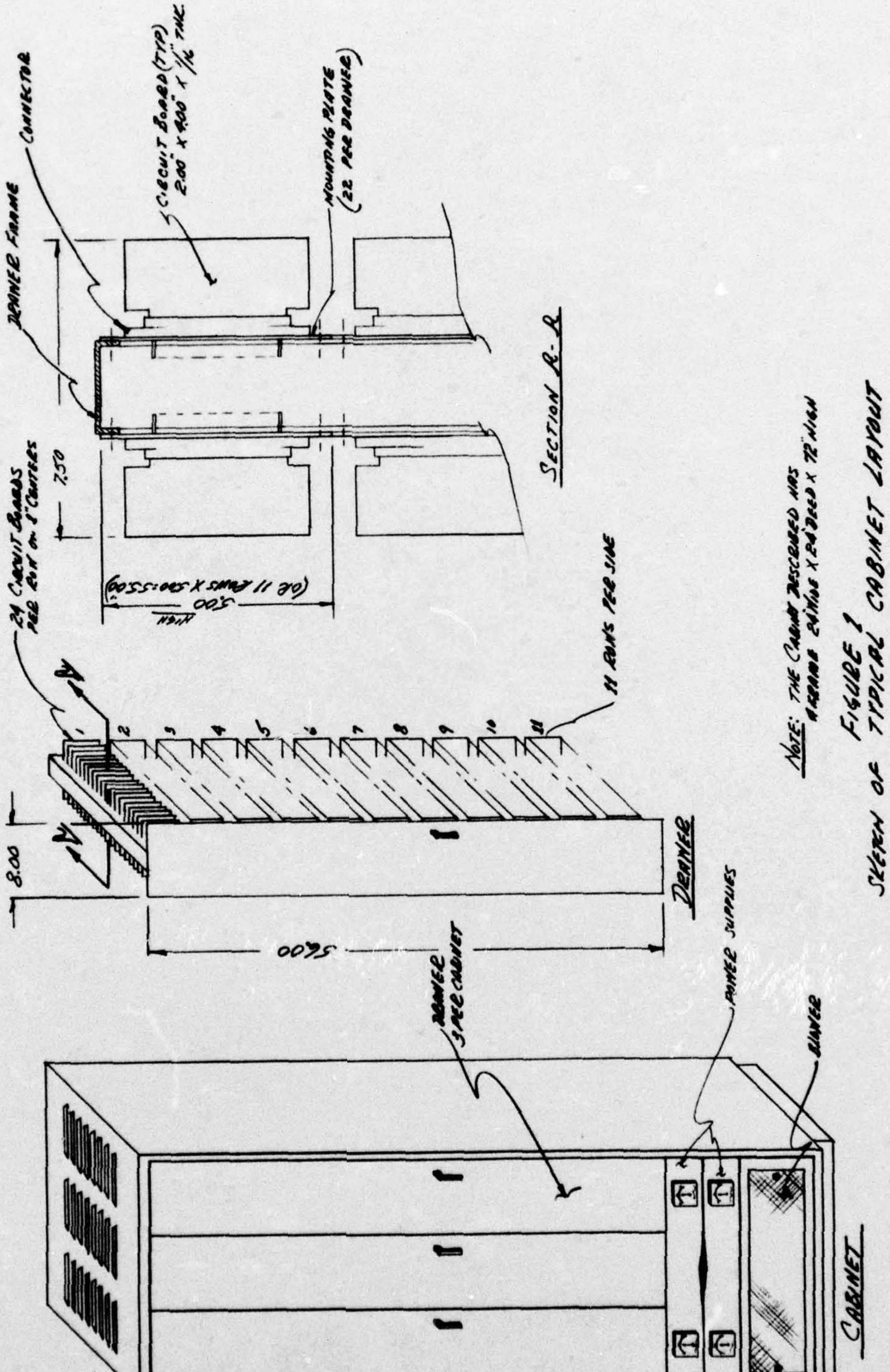

FIGURE 1
SKETCH OF TYPICAL CABINET LAYOUT

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FIGURE 2

SIGNAL PROCESSOR SUBSYSTEM COST

225 Beams	NB Pulse Length $\frac{1}{4}$ sec WB Bandwidth 50 cps WB - BT = 8 SD Bandwidth = 50 cps		NB Pulse Length $=\frac{1}{2}$ sec WB Bandwidth 100 cps BT = 8 SD Bandwidth = 100 cps		NB Pulse Length/Sec WB Bandwidth 200 cps WB BT = 8 SD Bandwidth = 200 cps	
	Cost	Cabinets	Cost	Cabients	Cost	Cabinets
NB Preprocessor	$450K	3	$450K	3	$450K	3
Scanned Filter & Auto Gate	90K	$2\frac{1}{2}$	125K	$2\frac{1}{2}$	180K	$2\frac{1}{2}$
Wideband Mode Selector	100K	$\frac{1}{2}$	100K	$\frac{1}{2}$	100K	$\frac{1}{2}$
Wideband Clipper Correlator	12K	$\frac{1}{4}$	16K	$\frac{1}{4}$	25K	$\frac{1}{2}$
Wideband Simple Pulse Processor	110K	1	110K	1	110K	1
Surface Duct SP Processor	180K	$1\frac{1}{2}$	180K	$1\frac{1}{2}$	180K	$1\frac{1}{2}$
TOTAL	942K	8.75	981K	8.75	1,045K	9

TABLE 3

SIGNAL PROCESSOR SUBSYSTEM COST

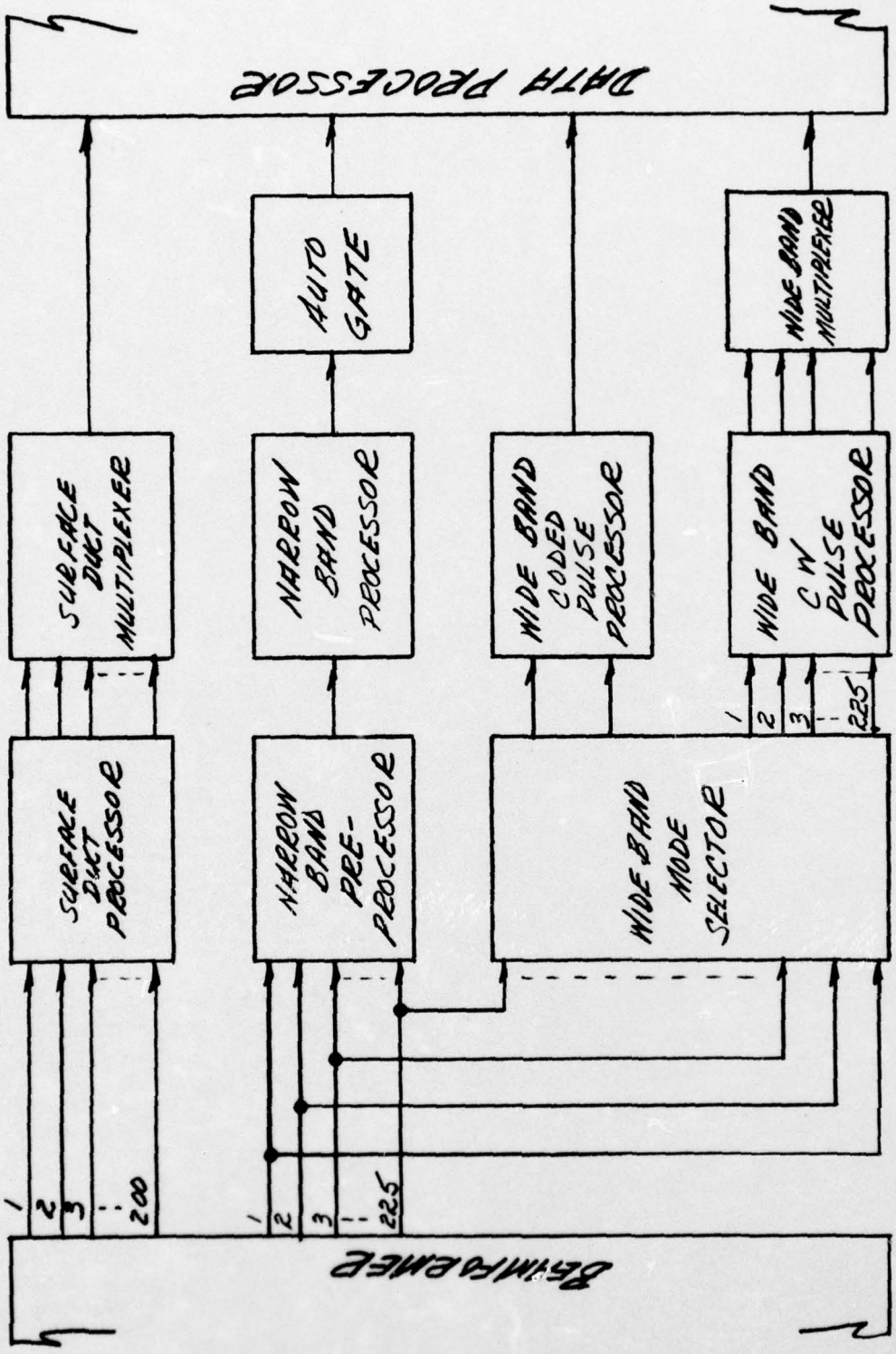

Figure 3. Signal Processor Subsystem Block Diagram

SECTION V

THE SURFACE DUCT PROCESSOR

A block diagram of the surface duct processor is shown in Figure 5. The 200 parrallel channel simple pulse processor shown corresponds to the system requirement assumed for the First Cut Signal Processor. It is assumed for costing purposes that this same configuration would be used for any combination of signal bandwidth within the range of 50 to 200 cps and number of beams in the range 100 to 1000. The First Cut Processor was designed for a 10 ms pulse and a sampling rate per beam of 400 cps was chosen as being adequate. In order to process 200 beams the time multiplexers in this case must operate at a 400 x 200 = 80 Kc rate which is well within the state-of-the-art and within the maximum data rate which is acceptable to the data processor. For the worst case situation of a 5 millisecond pulse and 1000 beams and a sampling rate of 800 cps per beam, the output data rate for this processor will be 800 x 1000 = 800 Kc. This data rate, although within the state-of-the-art is probably too high to be acceptable to the data processor. Therefore, if a processor were to be built for this case an implementation using four identical processors each capable of processing 250 beams would probably be used. However, the multiplexer cost also varies as a function of the number of beams, therefore the material costs would not be affected appreciably by this kind of implementation change.

For a particular number of beams within the 100 - 1000 range the processor material cost is not affected by a change in bandwidth from 50 cps to 200 cps.

Table 4 shows the cost estimate and number of cabinets as a function of number of beams for each of the blocks in Figure 5. The data presented in Table 4 was used to plot Figure 4 which shows cost and number of cabinets as a function of the number of beams to be processed.

Costs for this processor were based on the assumption that most of the equipment would be built in house. The total cost figures are therefore strongly influenced by the assumption that an average circuit board which would comprise one filter (for instance) would cost about $100 for materials, assembly and test.

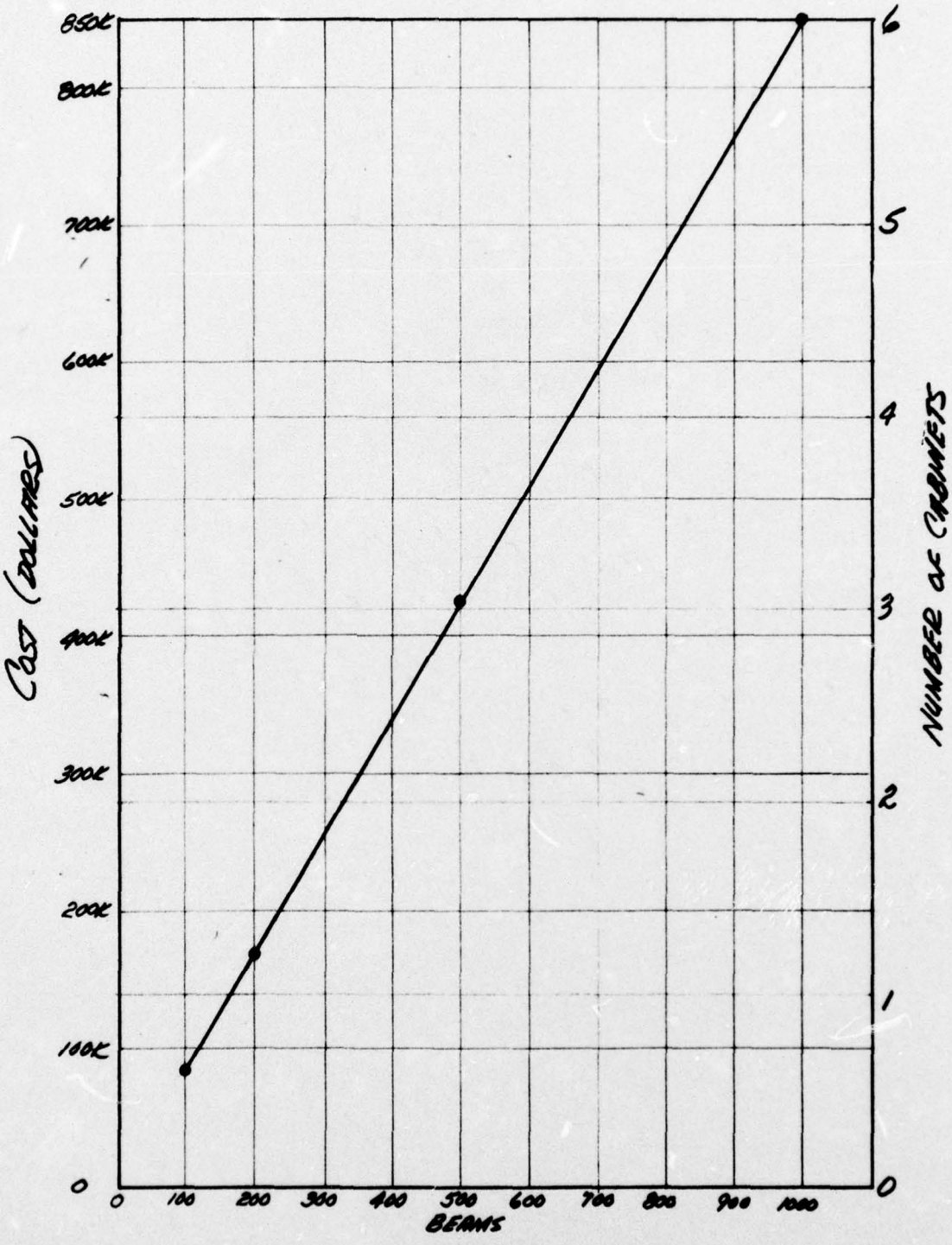

FIGURE 4
SURFACE DUCT PROCESSOR COST

SIMPLE PULSE PROCESSOR COST

BEAMS	FILTER		OVERLOAD LIMITER		ENVELOPE DETECTOR		LO-PASS FILTER		TOTAL BOARDS	CABINETS		TOTAL COST
NUMBER	BOARDS	COST	BOARDS	COST	BOARDS	COST	BOARDS	COST	NUMBER	COST	NUMBER	BOARDS & CAB.
100	300	$30K	100	$10K	200	$20K	100	$10K	700	$2K	1/2	$72K
200	600	60K	200	20K	400	40K	200	20K	1400	4.1K	1	144.1K
500	1500	150K	500	50K	1000	100K	500	50K	3500	10.3K	2 1/2	360.3K
1000	3000	300K	1000	100K	2000	200K	1000	100K	7000	20.6K	5	720.6K

TIME MULTIPLIXER COST

BEAMS	TIMING		GATE		SUMMER		DRIVER		TOTAL BOARDS	CABINETS		TOTAL COST
NUMBER	BOARDS	COST	BOARDS	COST	BOARDS	COST	BOARDS	COST	NUMBER	COST	NUMBER	BOARDS & CAB.
1	6	$1.3K	1	$100	1	$100	1	$100	9	—	—	—
10	6	1.3K	10	1K	2	200	1	100	19	—	—	—
100	15	2.8K	100	10K	6	600	1	100	122	.4K	1/8	13.9K
200	27	4.75K	200	20K	11	1.1K	1	100	239	.8K	1/4	26.75K
500	65	11K	500	50K	27	2.7K	1	100	593	2.0K	1/2	65.8K
1000	123	20.95K	1000	100K	52	5.2K	1	100	1176	4.1K	1	129.75K

TABLE 4

SURFACE DUCT PROCESSOR COST

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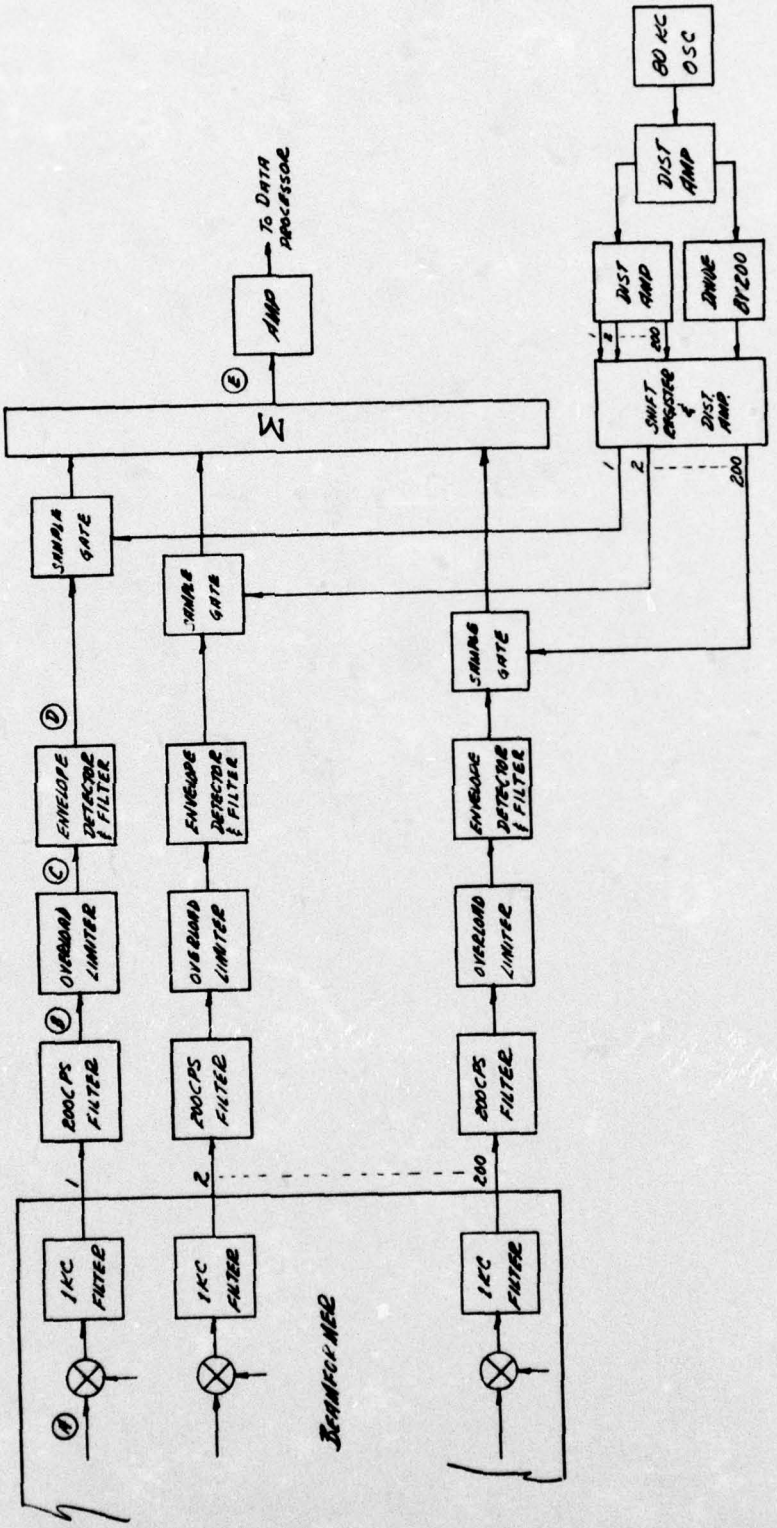


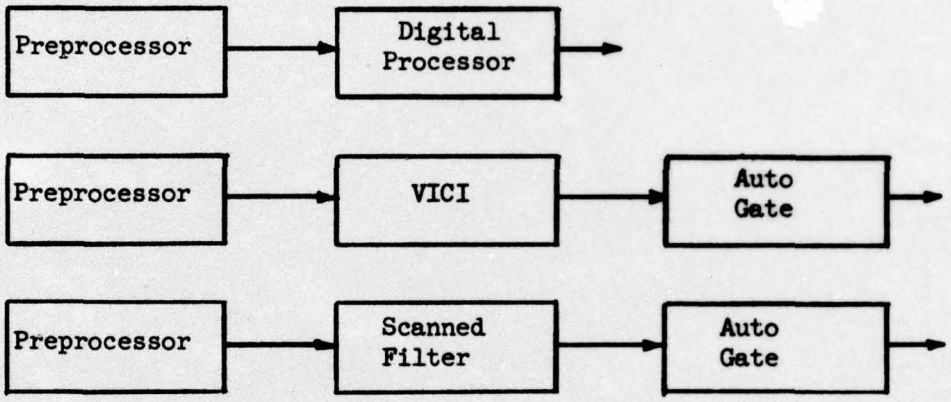
Figure 5. Block Diagram of the Surface Duct Processor

SECTION VI

THE NARROW BAND PROCESSOR

A. INTRODUCTION

Three Narrowband Processors were considered in the First Cut Signal Processing report. The major components of each is shown in the sketch below



Even though there are minor functional differences in the preprocessors for the three cases shown, the costs for any particular combination of pulse length and number of beams in the ranges considered are nearly the same. Therefore, for costing purposes the scanned filter preprocessor was costed in detail and the same cost figures were used for the other two preprocessors.

In all cases the general procedure for costing was to select particular combinations of number of beams and pulse width and to decide on system configurations for each of the combinations. The case of the digital VICI illustrates the procedure. Here pulse lengths of 1/4, 1/2 and 1 second and numbers of beams of 125, 250, 500 and 1000 were chosen in order to define twelve system configurations. For each system a judgement was made concerning whether to make a particular part more complex with increase in number of beams and/or pulse length or to split the function into two less complex parts.

B. THE NARROWBAND PREPROCESSOR

A block diagram of the preprocessor for the Scanned Filter is shown in Figure 7. The 225 channel case shown corresponds to the system requirement assumed for the First Cut Signal Processor. The requirements on individual components of the preprocessor do not change appreciably with change of signal pulse length in the range 1/4 to 1 sec. consequently the cost figures are independent of pulse length. The input filter, reverberation notch, range gate and sampling gate requirements are independent of the number of beams. However, the bandwidth of the gate generating circuitry and the multiplexer output bandwidth increases with increase in number of beams, therefore, in actual implementation a judgement would be required to determine for any particular application whether a single high bandwidth multiplexer or two or more lower bandwidth multiplexers should be used. It was assumed that this judgement would result in two or more multiplexers of the same or lower bandwidth as that required for the First Cut configuration. Therefore, number of components for the multiplexing and gate generating circuitry were assumed to vary linearly with number of beams. Since component costs were considered to be independent of number of identical components, the preprocessor costs are a linear function of the number of beams.

Table 5 summarizes the cost and number of cabinet estimates for each of the blocks in Figure 7. The data in Table 5 was used to plot Figure 6 which shows cost and number of cabinets as a function of number of beams to be processed.

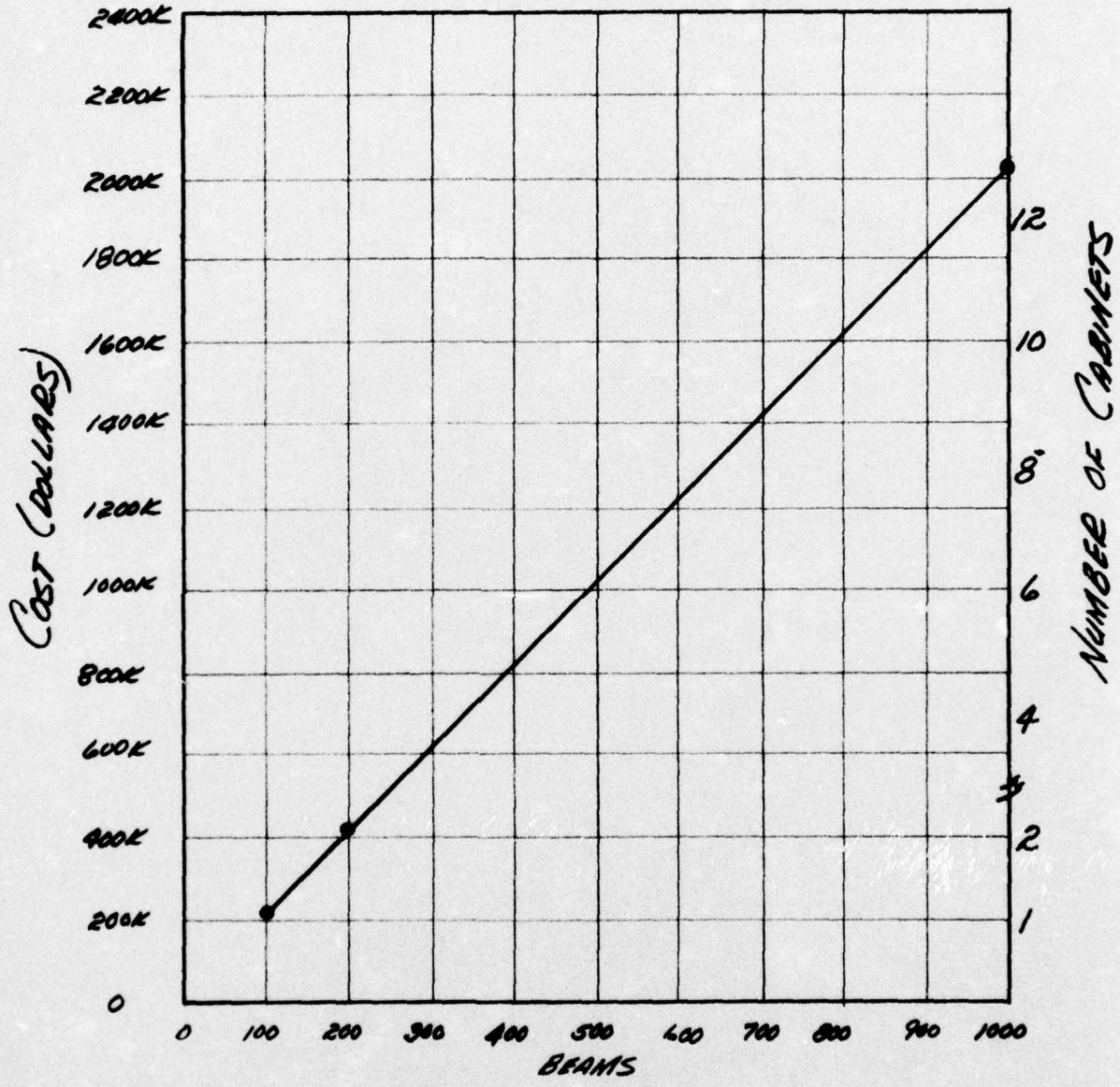


FIGURE 6

SCANNED FILTER PREPROCESSOR

TABLE 5

SCANNED FILTER PRE-PROCESSOR

BEAMS	TIMING		FILTER		ADAPTIVE EQUALIZER		SUMMER		RANGE & SAMPLE GATE		LOG AMP.		TOTAL BEAMS	CABINETS		TOTAL COST
NUMBER	BEAMS	COST	BEAMS	COST	BEAMS	COST	BEAMS	COST	BEAMS	COST	BEAMS	COST	NUMBER	COST	NUMBER	DOLLARS
100	15	$2.8K	200	$20K	1700	$170K	6	$600	100	$10K	1	$300	2021	$4.9K	1 1/4	$208.4K
200	27	13.5K	400	40K	3400	340K	11	1.1K	200	20K	1	300	4038	10.3K	2 1/2	44.9K
1000	123	20.35K	2000	200K	17000	1.70M	52	5.2K	1000	100K	1	300	20,182	51.3K	12 1/2	2.07M

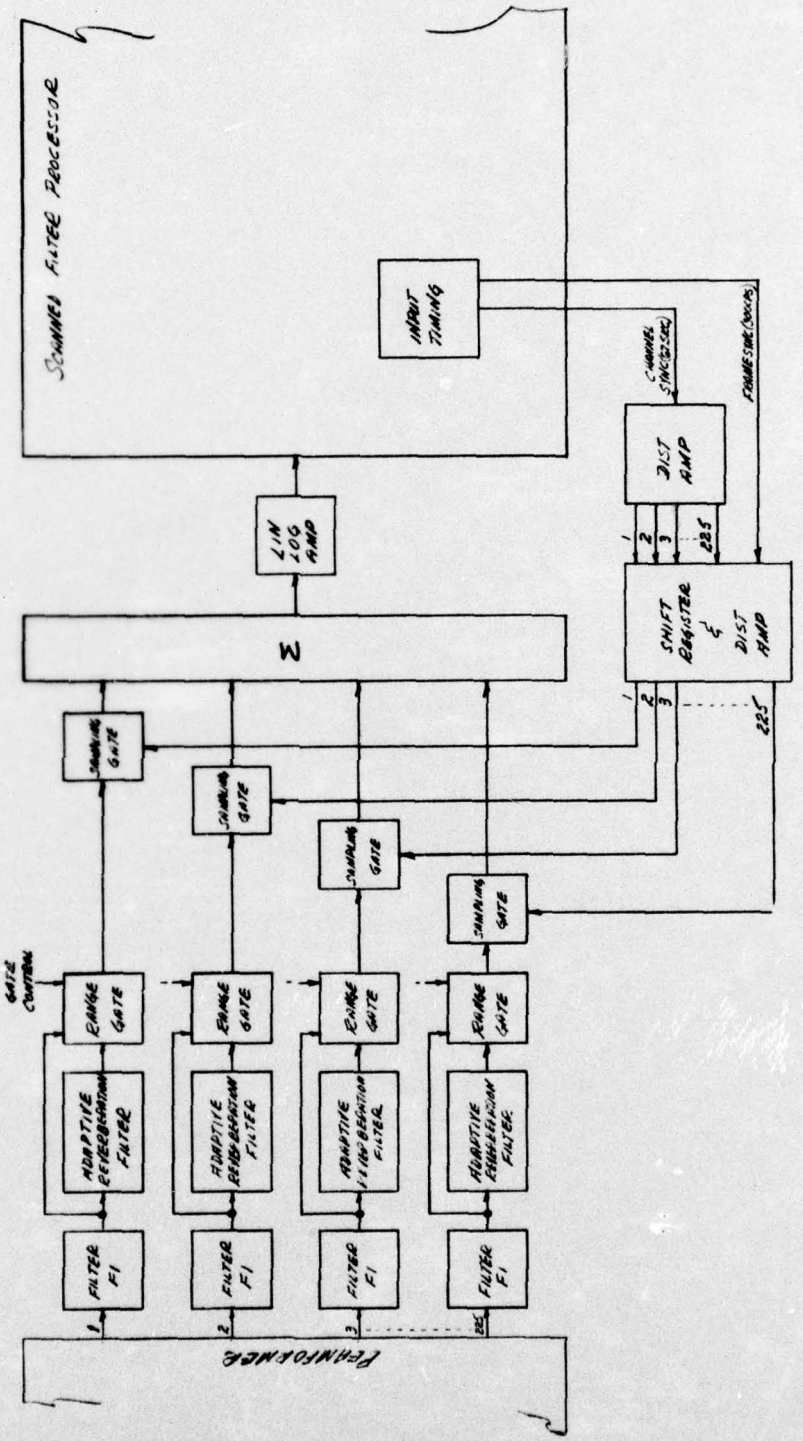


Figure 7. Block Diagram of the Scanned Filter Preprocessor

C. THE SCANNED FILTER AND AUTOGATE

The Scanned Filter and Auto Gate block diagrams for the 225 beam, 1/2 sec pulse requirement are shown in Figures 9 and 10. Twelve different Scanned Filter and Auto Gate processor configurations were studied in order to calculate costs. In general the designs of individual functions in these block diagrams were not appreciably changed with changes in number of beams and pulse length. Instead the number of identical functions required increases.

Tables 6 and 7 summarize the cost estimates made for the twelve scanned filter configurations studied and the Auto Gate. As can be seen from these tables the largest single cost item is the Magnetic Core memory.

The memory price for each configuration was costed on the basis of costs shown in the table below.

Memory Capacity	Cost/bit	Total Cost
2048 bits	$.24/bit	$ 35K
4096 bits	$.18/bit	$ 52K
8192 bits	$.15/bit	$ 87K
16384 bits	$.12/bit	$140K

In order to facilitate presentation of the memory cost in Table 6 the total memory cost figures were broken up into $5,000 units. The number of memory units required for each configuration was then inserted in the Table.

Figure 8 shows a plot of Scanned Filter costs as a function of number of beams for the three pulse widths considered.

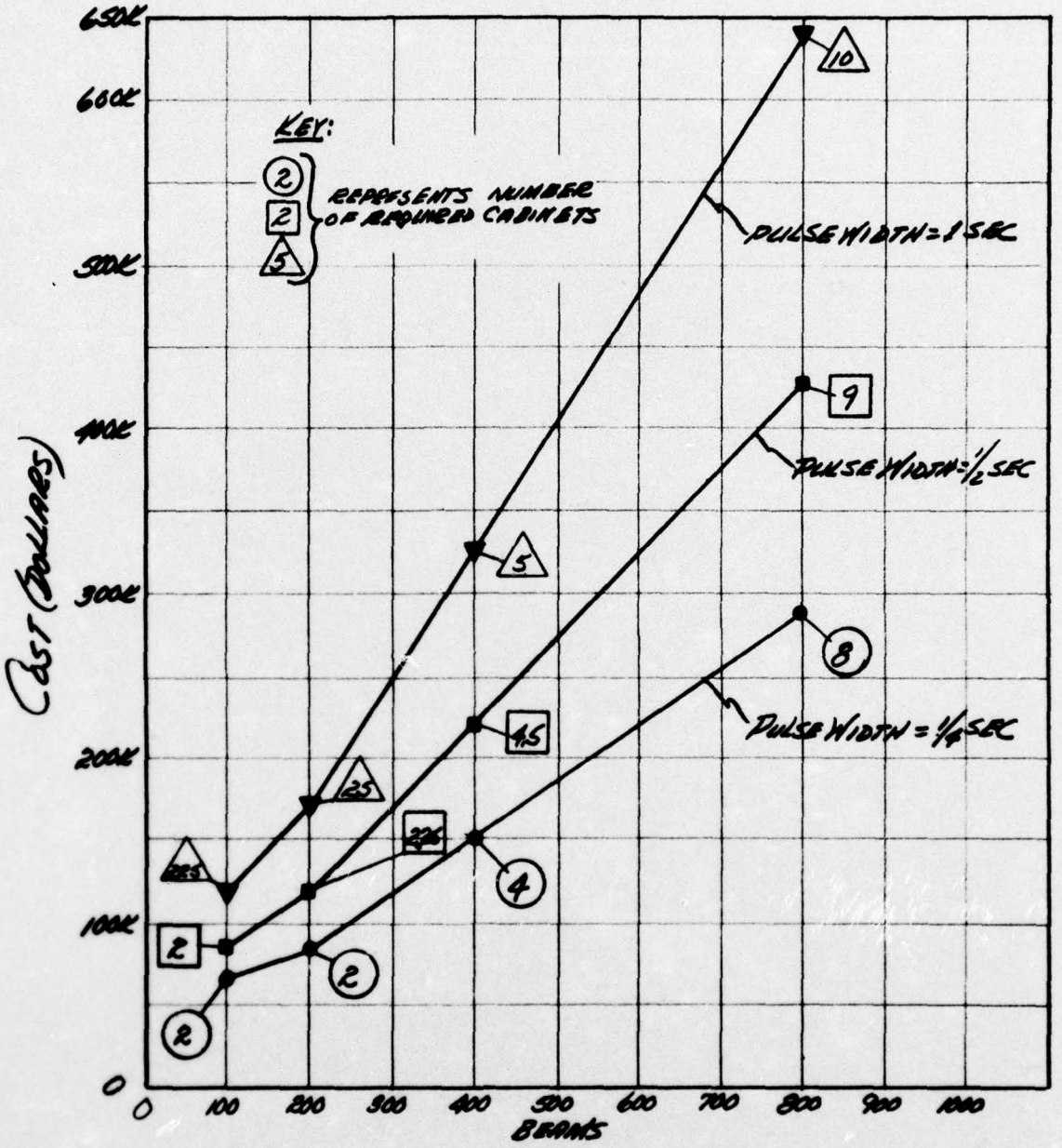


FIGURE 8

SCANNED FILTER & AUTOGATE COST

TABLE 6

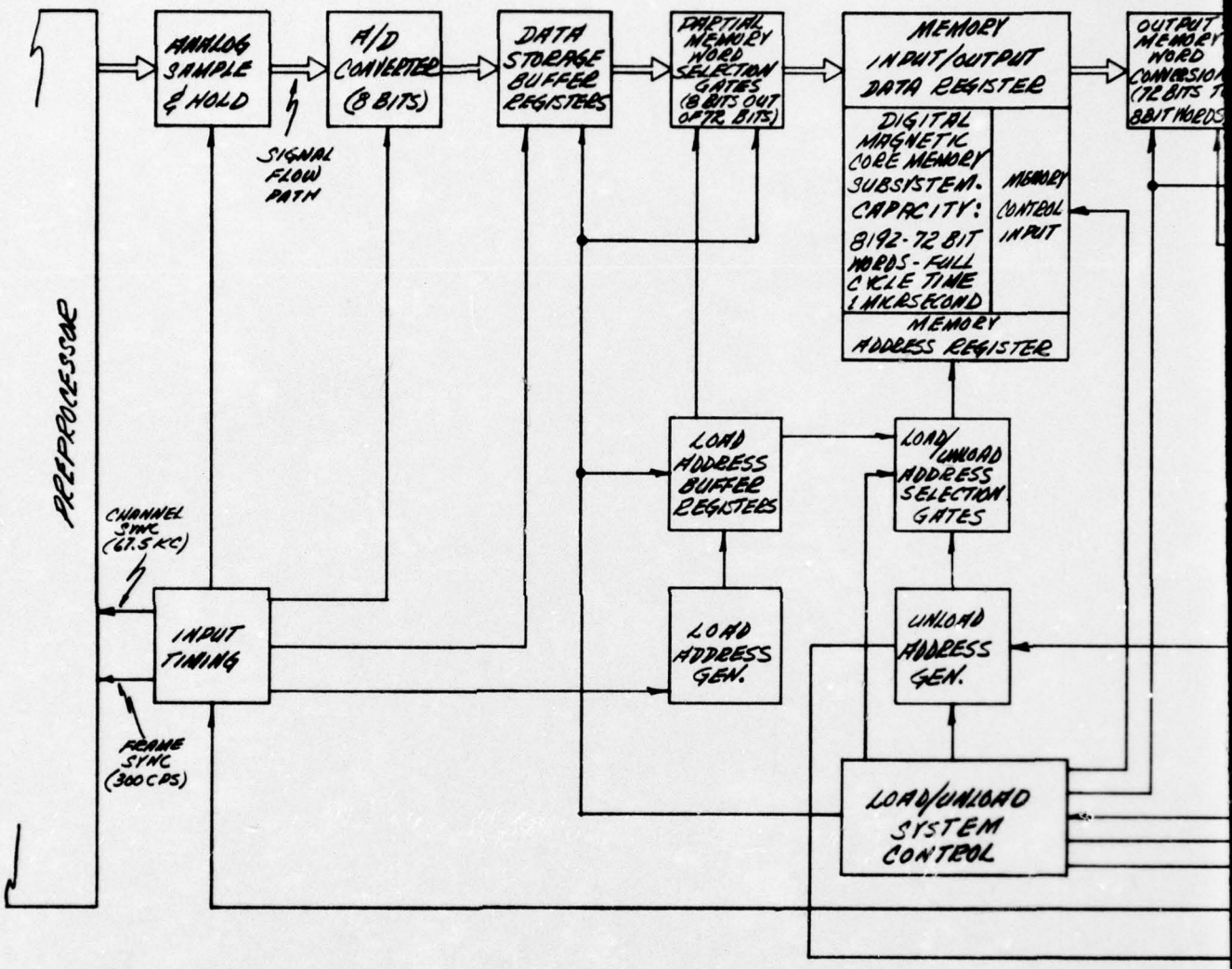
SCANNED FILTER & AUTO GATE COST

		NUMBER OF MODULES REQ.												COST PER MODULE
	No. Beams	100			200			400			800			
	Pulse Length (Sec)	1/4	1/2	1	1/4	1/2	1	1/4	1/2	1	1/4	1/2	1	
1.	Analog Sample and Hold													4.00K
2.	Analog/Digital Converter													7.00K
3.	Temporary Data Storage Buffer Registers	1	1	1	1	1	1	2	2	2	4	4	4	0.72K
4.	Partial Memory Word Selection Gates													2.16K
5.	Input Timing													1.08K
6.	Load Address Buffer Registers													1.35K
7.	Load Address Generator													3.60K
8.	Load/Unload Address Selection Gates	1	1	1	1	1	1	1	1	1	1	1	1	0.54K
9.	Load/Unload System Control													1.08K
10.	Unload Address Generator													1.80K
11.	Load/Unload Timing													1.80K
12.	System Clock Generator													0.36K
13.	Memory Register	7	10	17	10	17	28	21	35	56	42	70	112	5.00K
14.	Output Memory Word Conversion	1	1	1	1	1	1	2	2	2	4	4	4	1.44K
15.	Digital/Analog Converter													3.00K
16.	Signal Spectrum Bandpass Filter													0.20K
17.	Video Drive Amplifier													0.10K
18.	Balanced Mixer													0.25K
19.	Narrow Bandpass Pre-Detection IF Filter	1	1	1	1	1	1	2	2	2	4	4	4	0.40K
20.	IF Amplifier													0.40K
21.	Linear Envelope Detector													0.20K
22.	Low Pass Post-Detection Filter													0.10K
23.	Peak Detection and Hold Circuit													0.25K
24.	Oscillator Drive Amplifier													0.20K
25.	Voltage Controlled Step Scan Oscillator													0.50K
26.	Digital Step Scan Generator	1	1	1	1	1	1	1	1	1	1	1	1	0.90K
27.	Filter Delay Compensation													0.60K
28.	Auto Gate	1	1	1	1	1	1	2	2	2	4	4	4	3.00K

Tapped Delay Line	$1,000
Delay Line & Associated Circuits	1,300
Distribution Amplifier	300
Gain Controlled Amplifier	300
Comparator	300
Summer	200
Gate Generator	200
Gate	100
	$3,700

TABLE 7

AUTO GATE COST


PREPROCESSOR
ANALOG SAMPLE & HOLD
A/D CONVERTER (8 BITS)
SIGNAL FLOW PATH
DATA STORAGE BUFFER REGISTERS
PARTIAL MEMORY WORD SELECTION GATES (8 BITS OUT OF 72 BITS)
MEMORY INPUT/OUTPUT DATA REGISTER
DIGITAL MAGNETIC CORE MEMORY SUBSYSTEM. CAPACITY: 8192-72 BIT WORDS - FULL CYCLE TIME 1 MICROSECOND
MEMORY CONTROL INPUT
MEMORY ADDRESS REGISTER
OUTPUT MEMORY WORD CONVERSION (72 BITS T
8 BIT WORDS
CHANNEL SYNC (67.5 KC)
INPUT TIMING
FRAME SYNC (300 CPS)
LOAD ADDRESS BUFFER REGISTERS
LOAD ADDRESS GEN.
LOAD/UNLOAD ADDRESS SELECTION GATES
UNLOAD ADDRESS GEN.
LOAD/UNLOAD SYSTEM CONTROL

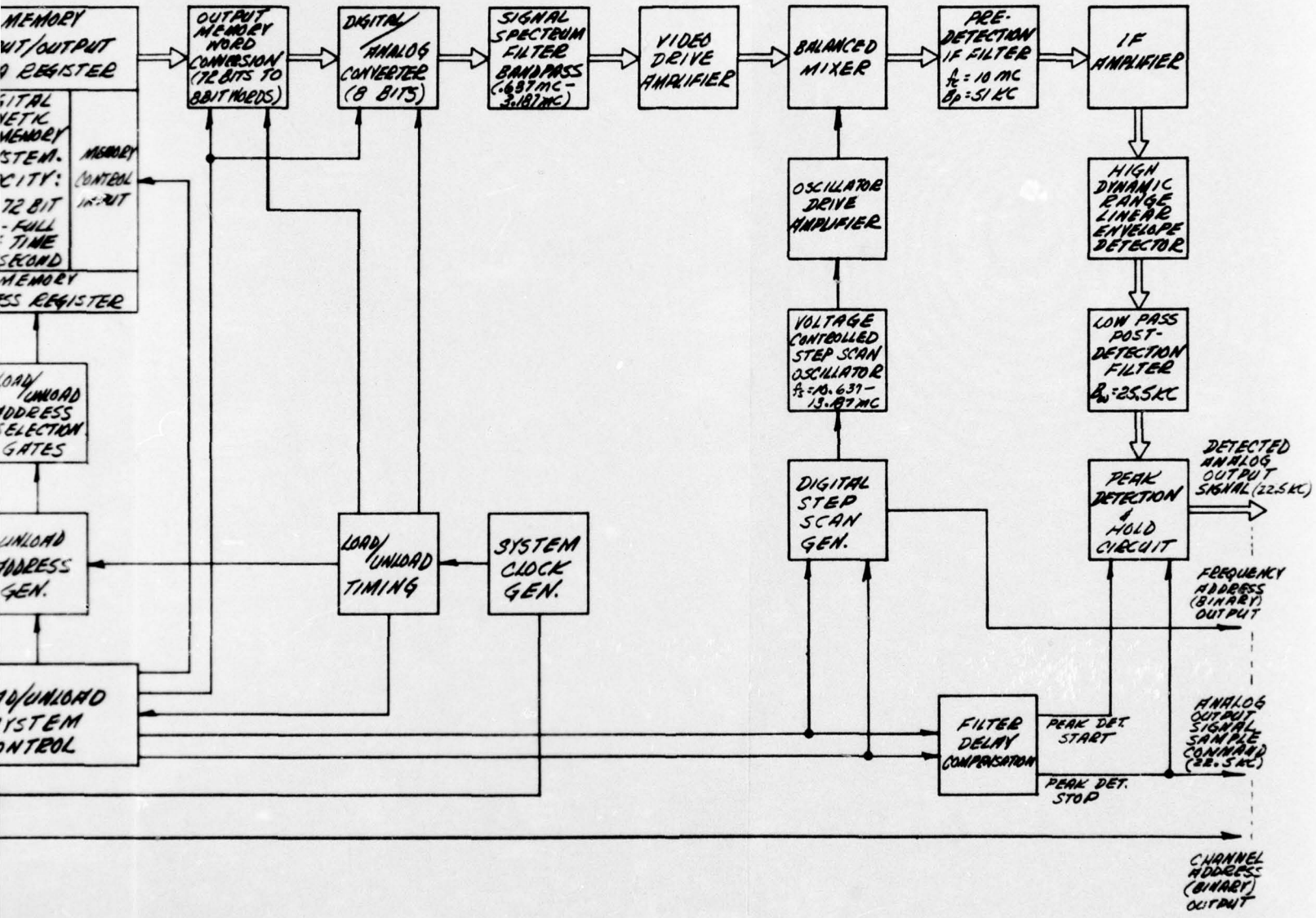


Figure 9. Detailed Block Diagram of the Scanned Filter

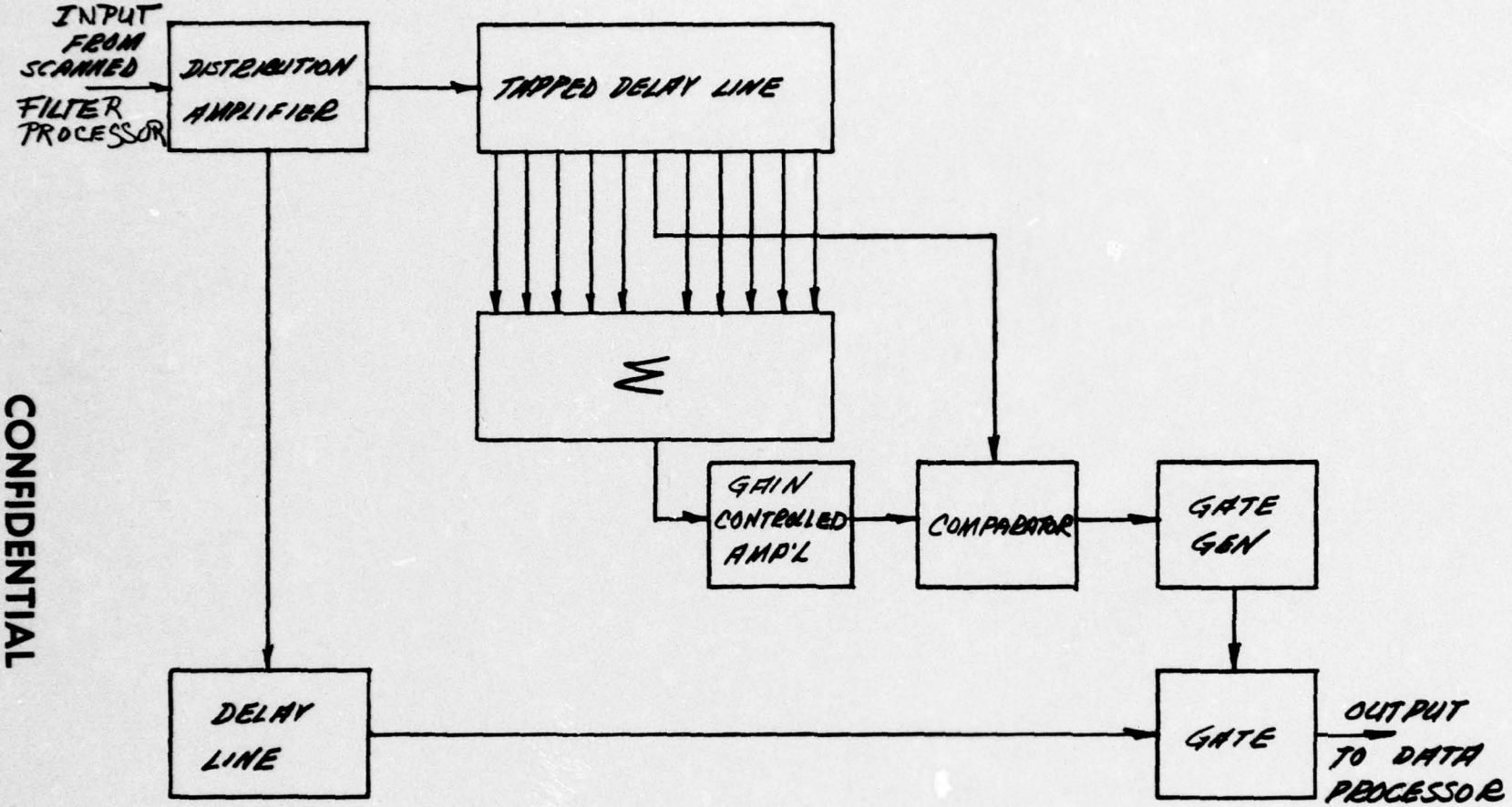


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Figure 10. Block Diagram of the Auto Gate

D. THE VICI PROCESSOR AND AUTO GATE

A block diagram of the VICI processor is shown in Figure 13. This same configuration would be used for any combination of pulse length within the range 1/4 to 1 sec and number of beams in the range 100 to 1000. However, in cases where a given combination of pulse length and number of beams is beyond the capabilities of a single VICI, two or more VICI's are required in parallel.

Figure 11 shows the trade-off that must be considered in choosing a VICI for a particular pulse length and number of beams. A point on this curve represents the desired operating point in terms of pulse length and number of beams. The lines of constant BT product show the time-bandwidth requirement on the VICI delay line and the lines of constant dynamic range shows the performance to be expected from the processor. The dashed line represents the desired operation contour.

If we were to choose an operating point to the right of the dashed line, the time bandwidth requirement for the delay line begins to get excessive, such that design problems increase very rapidly. In fact BT products in the range 20 to 25 are pushing the quartz delay line state-of-the-art. Therefore an operating point too far to the right of the operational contour represents a requirement that is beyond the state-of-the-art for a single VICI. If we pick an operating point to the left of the dashed curve the VICI design problems become less severe. However, an operating point too far to the left indicated that the full capacity of the VICI is not being used.

Table 8 shows the cost break down for a single VICI. This table used in conjunction with Figure 11 to determine the number of VICI's required for a particular pulse width allows one to calculate cost versus number of beams. In order to estimate number of cabinets it was assumed that four VICI processors can be packaged in a single cabinet.

Figure 12 shows a plot of the resulting cost and number of cabinets as a function of number of beams for several pulse lenghts.

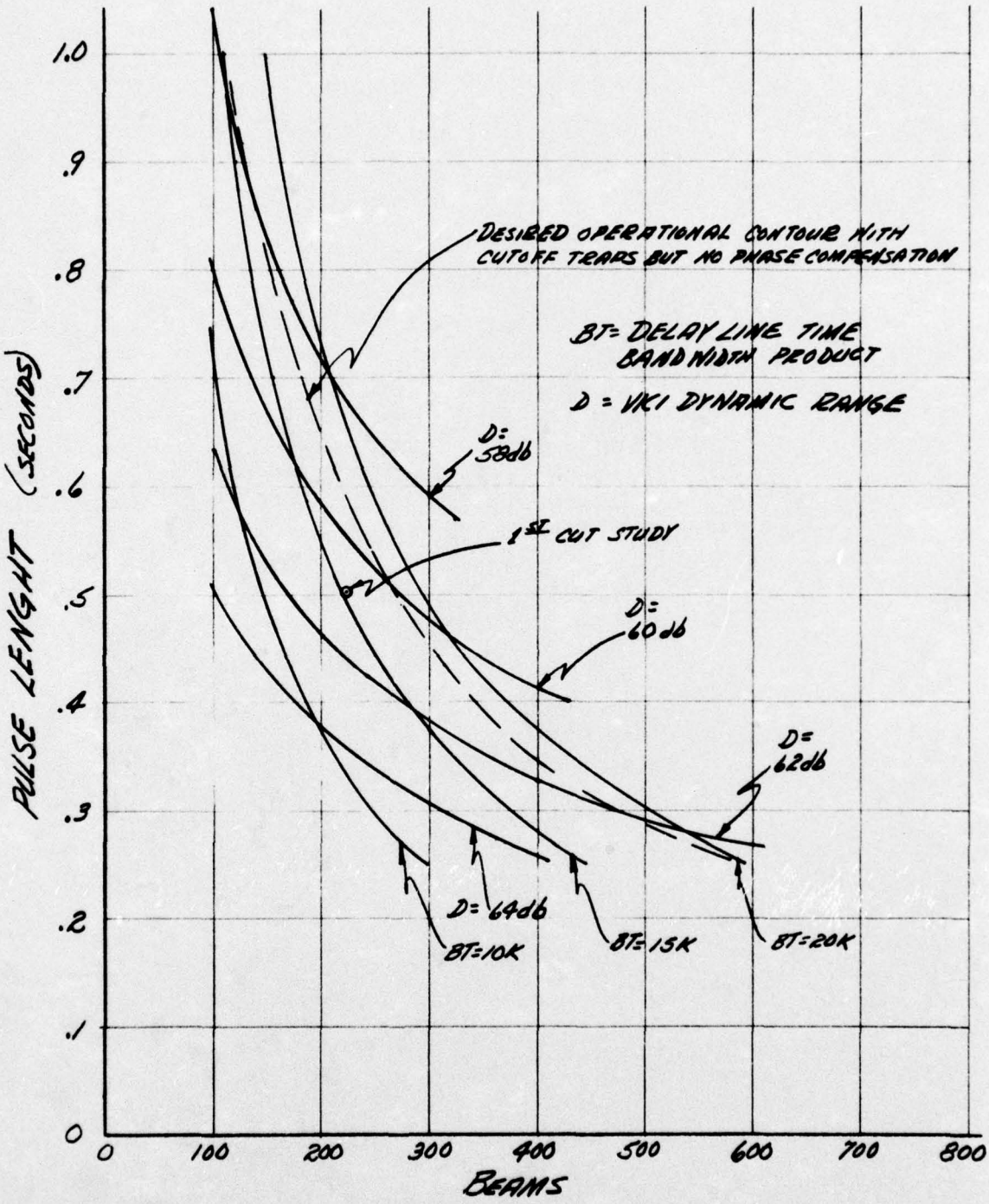

FIGURE 11
VICI OPERATIONAL CONTOUR

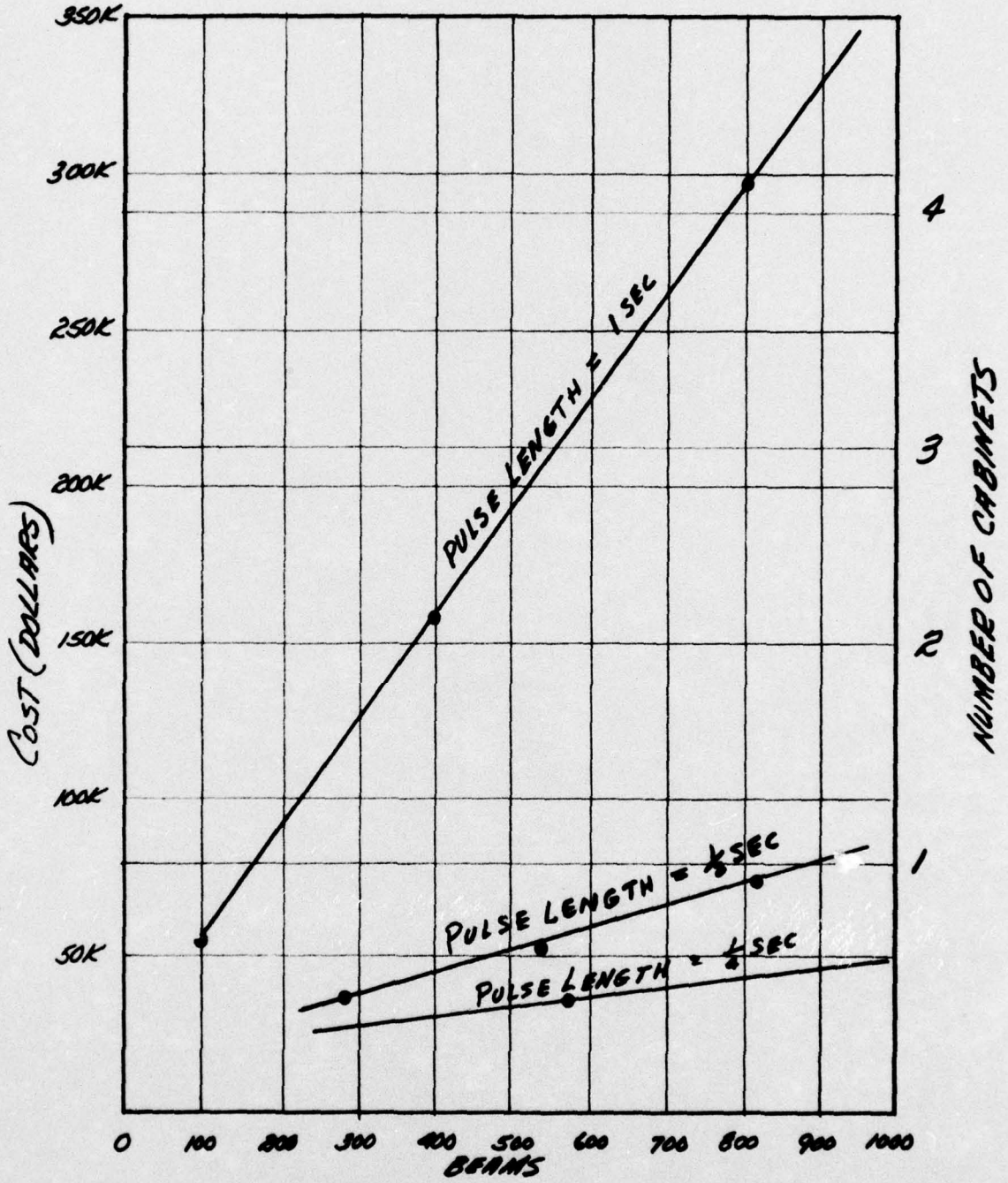

FIGURE 12

VK1 & AUTOGATE COST

(2)	Delay Lines	$7,000
(2)	Delay Line Drivers	400
(2)	Post Delay Amplifiers	200
	Upshifter & L.O.	1,200
	Downshifter & L.O.	1,200
	AGC Control	1,500
	f_s Gen. & Phase Det.	1,500
	Variable Gain	100
	T.P. Gain & Summer	200
*	Cabinet, Power Supplies & Misc.	1,000
		$14,300

TABLE 8

VICI COST

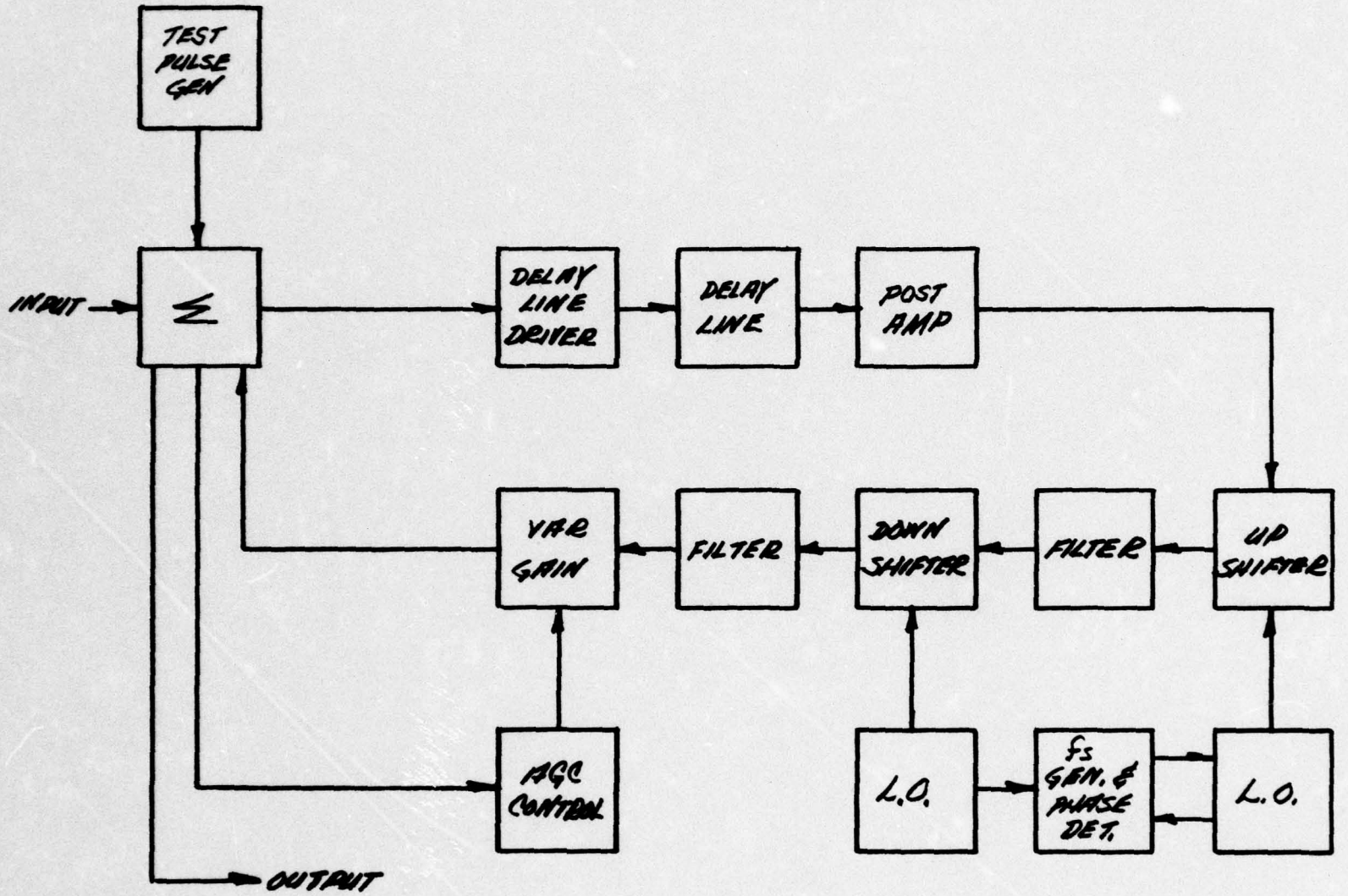

Figure 13. VICI Block Diagram

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E. THE DIGITAL DOPPLER PROCESSOR

The basic Digital Doppler Processor costed here is described in a memo entitled "Application of a Digital Signal Processor to the Planar Array Sonar".[5] A block diagram for the 225 beam, 1/2 sec pulse requirement is shown in Figure 15.

As described in the introduction to this Section, twelve different configurations covering the desired ranges of pulse length and number of beams were studied in order to estimate cost and number of cabinets required.

Table 9 shows a cost break down referenced to the block diagram in Figure 15.

Table 10 shows some of the important system parameters for each of the configurations costed.

A plot of cost and number of cabinets as a function of number of beams for several pulse lengths is given in Figure 14.

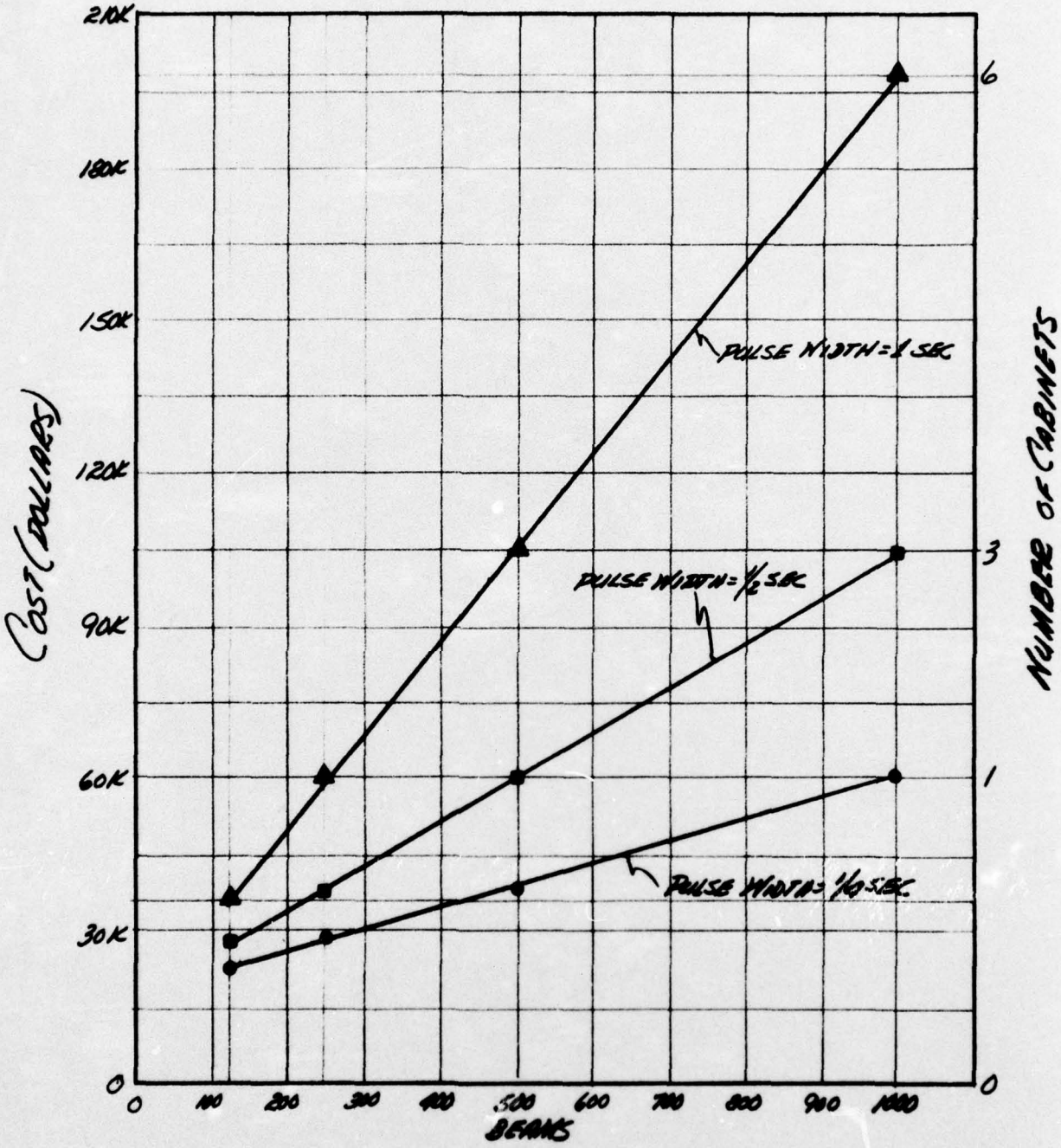


FIGURE 14
DIGITAL PROCESSOR COST

TABLE 9

DIGITAL PROCESSOR COST

(IN THOUSANDS OF DOLLARS)

# BEAMS	125			250			500			1000		
PULSE LENGTH (SEC)	1/4	1/2	1	1/4	1/2	1	1/4	1/2	1	1/4	1/2	1
1. SYNC. DET.	$ 1.5	1.5	1.5	2.0	2.0	2.0	2.5	2.5	2.5	3.0	3.0	3.0
2. 90° PHASE SHIFT	$ 0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1
3. SAMPLE & HOLD	$ 0.4	0.4	0.4	0.5	0.5	0.5	0.7	0.7	0.7	1.0	1.0	1.0
4. A/D CONVERTER	$ 4.0	4.0	4.0	5.0	5.0	5.0	6.0	6.0	6.0	8.0	8.0	8.0
5. PAR-TO-SER. CONV.	$ 0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.3	0.2	0.3	0.3
6. MULTIPLIER QUAD.	$ 2.0	2.5	3.0	2.5	3.0	6.0	3.0	6.0	12.0	6.0	12.0	24.0
7. CORE INTEG. STORE	$20.0	30.0	40.0	30.0	40.0	80.0	40.0	80.0	160.0	80.0	160.0	320.0
8. INTEGRATOR ADDERS	$ 0.3	0.3	0.3	0.3	0.3	0.6	0.3	0.6	1.2	0.6	1.2	2.4
9. MAGNITUDE PROC.	$ 2.0	2.5	3.0	2.5	3.0	3.2	3.0	3.2	3.4	3.2	3.4	3.8
10. WEIGHT. MULT.	$ 1.0	1.1	1.3	1.1	1.3	2.6	1.3	2.6	5.2	2.6	5.2	10.4
11. WEIGHT STORE	$ 0.5	0.7	1.0	0.5	0.7	1.1	0.5	0.8	1.4	0.6	1.1	1.9
12. RECIRC. STORE	$ 0.2	0.2	0.2	0.2	0.2	0.4	0.2	0.4	0.8	0.4	0.8	1.6
13. S/C STORE	$ 0.6	1.2	2.5	0.8	1.5	5.0	1.0	3.0	10.0	2.0	6.0	20.0
14. DIGITAL CLOCK	$ 1.5	2.0	3.0	2.0	3.0	5.0	3.0	5.0	9.0	5.0	9.0	18.0
15. CONTROL & TIMING	$ 2.5	3.5	5.0	3.5	5.0	8.5	5.0	8.5	15.0	8.5	15.0	30.0
16. POWER SUPPLIES	$ 2.5	2.8	3.0	2.8	3.0	4.0	3.0	4.0	6.0	4.0	6.0	10.0
Less items 14,15,16	$32.8	44.7	57.5	45.7	57.8	106.7	58.8	106.1	203.6	107.7	202.1	396.5
Less items 14,15,16 & 7	$15.8	19.2	25.5	20.2	25.8	42.7	26.8	42.1	75.6	43.7	74.1	140.5
Sub-Total Items 14,15,16	$ 6.5	8.3	11.0	8.3	11.0	17.5	11.0	17.5	30.0	17.5	30.0	58.0
Total (less item 7)	$22.3	27.5	36.5	38.5	36.8	60.2	37.8	59.6	105.6	61.2	104.1	198.5

NO. BEAMS	125	250	500	1000
Pulse Length (Sec)	$\frac{1}{4}$ $\frac{1}{2}$ 1	$\frac{1}{4}$ $\frac{1}{2}$ 1	$\frac{1}{4}$ $\frac{1}{2}$ 1	$\frac{1}{4}$ $\frac{1}{2}$ 1
Input Word Rate Kc	12 Kc	24 Kc	48 Kc	96 Kc
Processor Word Rate Mc	0.29 0.58 1.15	0.58 1.15 2.30	1.15 2.30 4.60	2.30 4.60 9.22
Number of Quads	1 1 1	1 1 2	1 2 4	2 4 8
Quad Bit Rate (Mc)	3.5 6.9 13.8	6.9 13.8 13.8	13.8 13.8 13.8	13.8 13.8 13.8
Integrator Store (#12 bit words)	6K 12K 24K	12K 24K 48K	24K 48K 96K	48K 96K 192K

TABLE 10

DIGITAL PROCESSOR PARAMETERS

DIGITAL DOPPLER PROCESSOR FLOW DIAGRAM

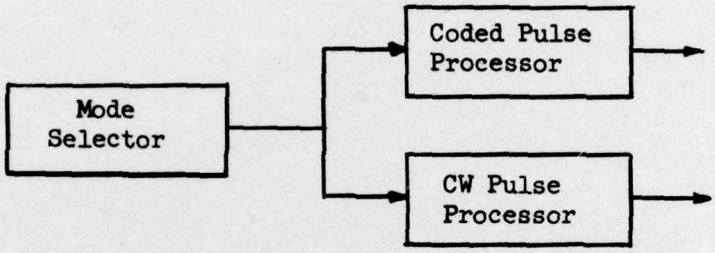
FIGURE 15

SECTION VII

THE WIDEBAND PROCESSOR

A. INTRODUCTION

A block diagram showing the major components of the wideband processor is shown below.



For the range of signal bandwidths from 50 - 200 cps and BT products of 1 to 12, the coded pulse processor costs vary as a function of bandwidth, BT product and number of beams. The mode selector and CW pulse processor costs vary only as a function of number of beams. The wideband CW pulse processor is identical to the surface duct processor except for the input filter which is contained in the mode selector. Since the CW pulse processor costs are detailed in Section V, only the mode selector and coded pulse processor costs will be presented here.

The technique for handling more beams, higher BT products and larger bandwidths for the Mode Selector and the Coded Pulse processor is to add parallel functions rather than making functions more sophisticated.

B. THE MODE SELECTOR

A detailed block diagram of the Mode Selector is shown in Figure 17. Component costs and number of 2" x 4" circuit boards for various numbers of beams referenced to this figure are shown in Table 11.

The resulting Mode Selector costs and number of cabinets as a function of number of beams are plotted in Figure 16.

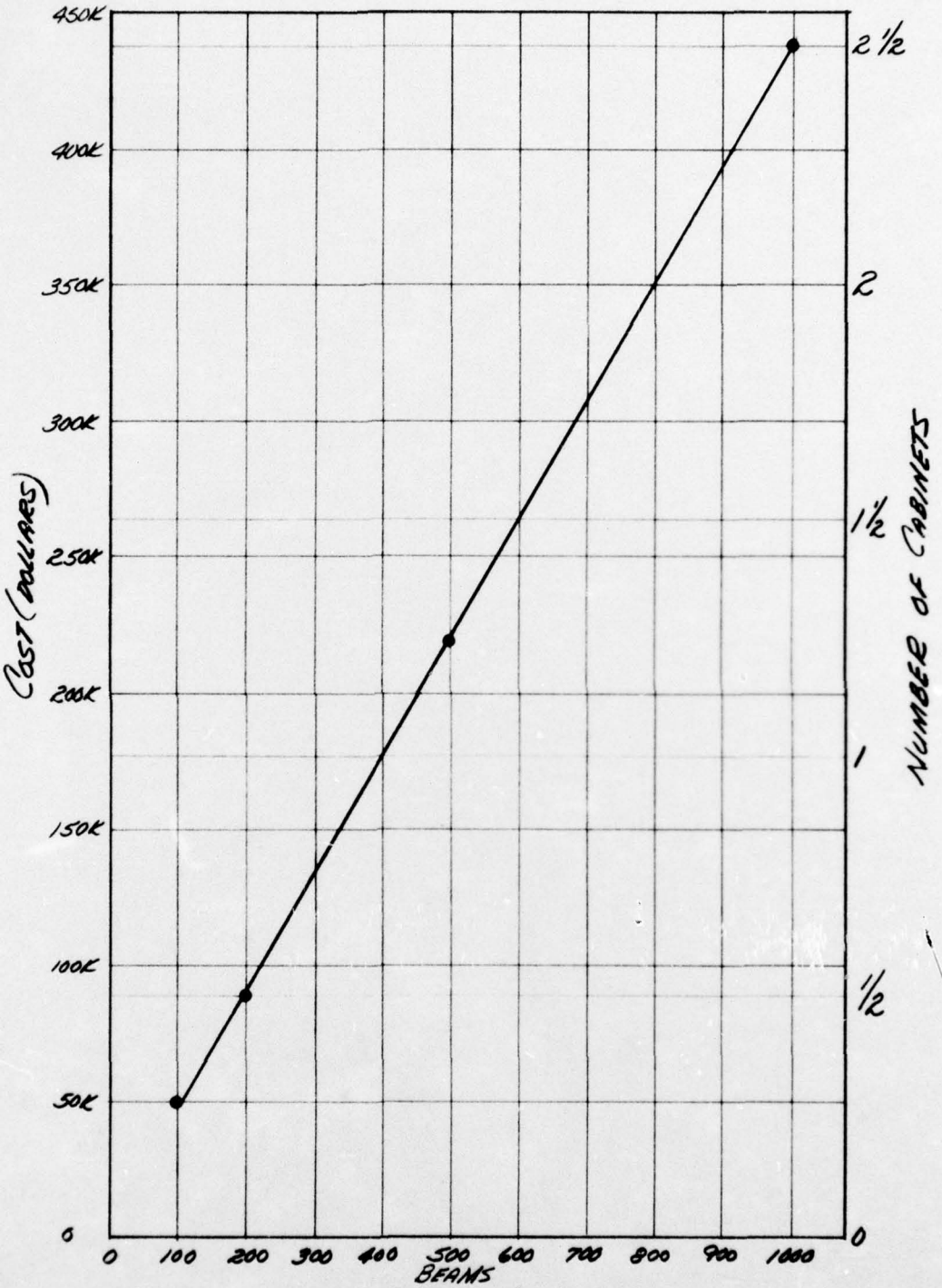
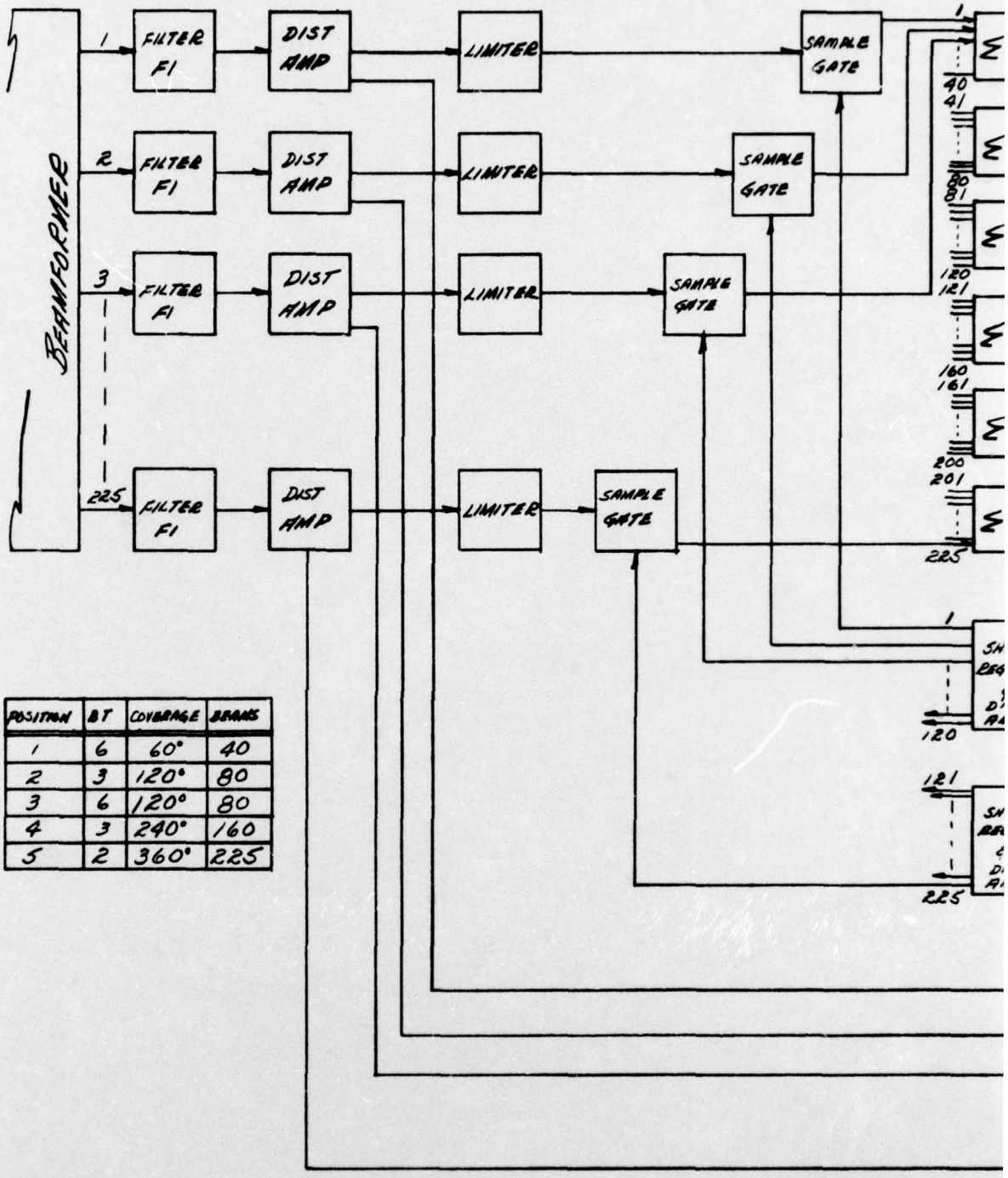


FIGURE 16
WIDE BAND MODE SELECTOR

TABLE II
WIDE BAND MODE SELECTOR COST

BEAM	TIMING		DIST AMP & FILTER		LIMITER & GATE		SUMMER		TOTAL BOARDS	CABINETS		TOTAL COST
NUMBER	BOARDS	COST	BOARDS	COST	BOARDS	COST	BOARDS	COST	NUMBER	COST	NUMBER	BOARDS & CAB.
100	20	$3.9K	200	$20K	100	$20K	6	$600	326	10K	1/4	44.9K
200	32	5.25K	400	40K	200	40K	11	1.1K	643	2.0K	1/2	88.35K
500	64	10.425K	1000	100K	500	100K	26	2.6K	1590	6.1K	1 1/4	218.2K
1000	128	20.85K	2000	200K	1000	200K	52	5.2K	3180	12.2K	2 1/2	438.25K



POSITION	BT	COVERAGE	BEAMS
1	6	60°	40
2	3	120°	80
3	6	120°	80
4	3	240°	160
5	2	360°	225

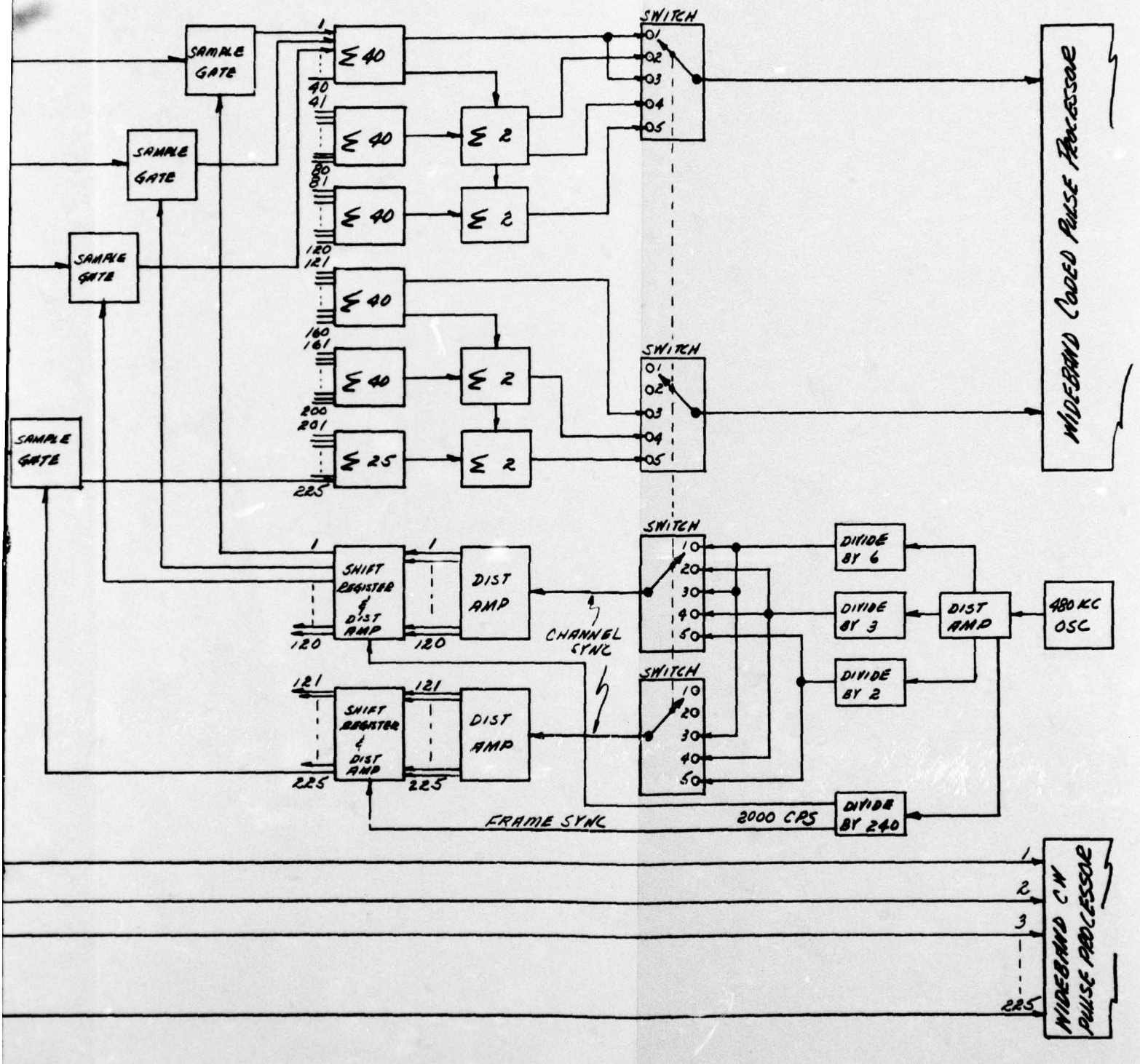


Figure 17. Wideband Mode Selector Block Diagram

C. THE CLIPPER CORRELATOR PROCESSOR

A block diagram of the clipper correlator processor is shown in Figure 19. The configuration shown meets the requirements assumed for the First Cut Signal Processor.

The First Cut Processor had the flexibility of choosing several different combinations of signal pulse length and number of beams for a 100 cps bandwidth coded pulse. In view of the fact that the clipper correlator configuration varies as a function not only of bandwidth and number of beams but also as a function of BT product it was decided to eliminate the switching flexibility for the purposes of costing.

Therefore, a number of processor configurations were studied, each configuration defined by pulse width, BT product, and number of beams to be processed. Table 12 shows the various combinations that were considered and specifies the number of "basic processors" needed for each configuration. Table 13 shows the "basic processor" cost with reference to Figure 19.

Curves of cost as a function of number of beams, BT product and Bandwidth were derived from Tables 12 and 13 and are presented in Figure 18.

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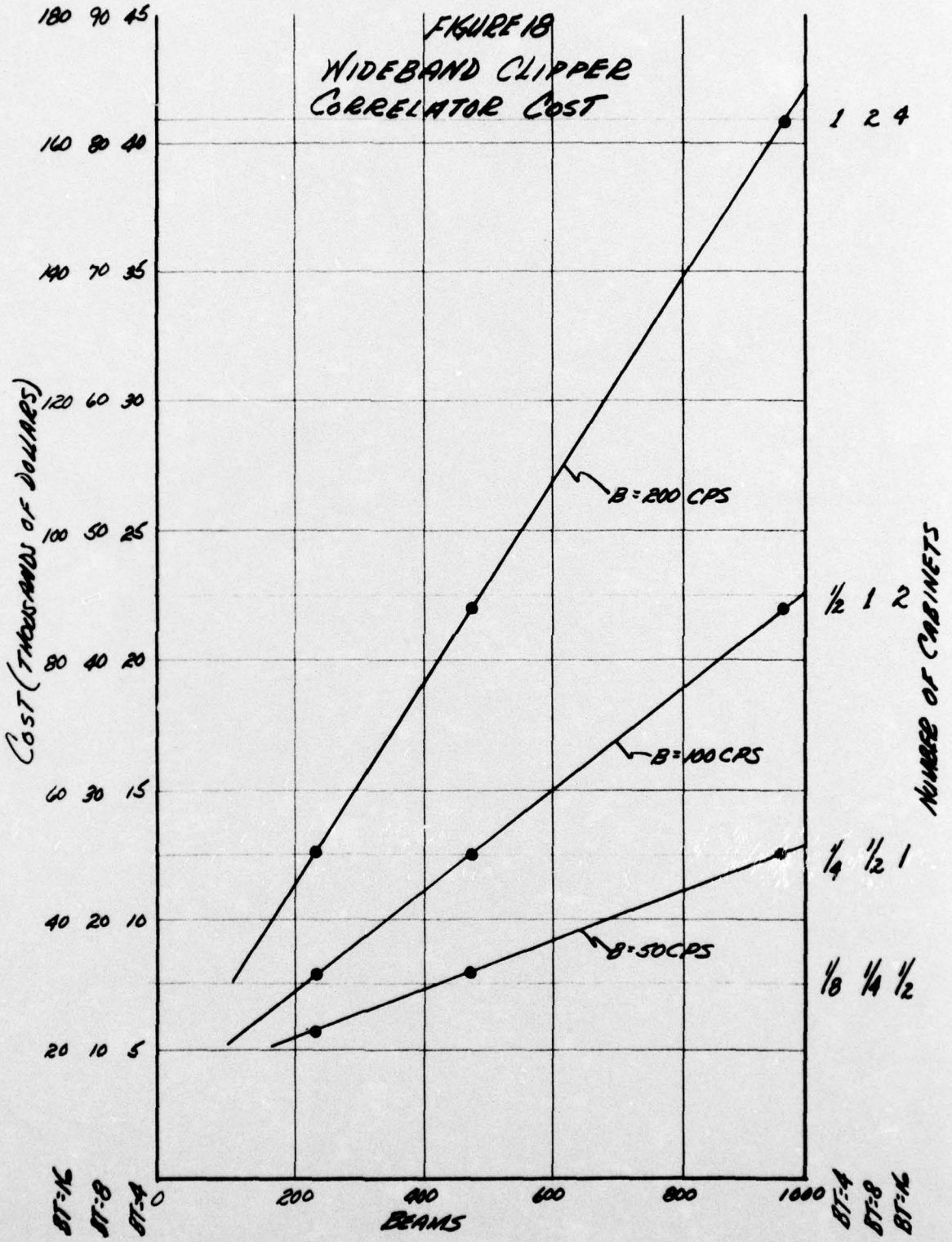
FIGURE 18
WIDEBAND CLIPPER
CORRELATOR COST
COST (THOUSANDS OF DOLLARS)
180 90 45
160 80 40
140 70 35
120 60 30
100 50 25
80 40 20
60 30 15
40 20 10
20 10 5
B=200 CPS
B=100 CPS
B=50 CPS
1 2 4
½ 1 2
¼ ½ 1
⅛ ¼ ½
NUMBER OF CABINETS
BT=16
BT=8
BT=4
0
200
400
600
800
1000
BEAMS
BT=4
BT=8
BT=16

f_s = 2000 cps 4800 bit capacity		NO. OF "BASIC" CLIPPER CORRELATOR PROCESSORS										
BT (For B = 50 cps)		2	4	8	12	16	24	32	36	40	48	56
BT (For B = 100 cps)			2	4	6	8	12	16	18	20	24	28
BT (For B = 200 cps)				2	3	4	6	8	9	10	12	14
Number of Beams	80						1				2	
	160				1		2		3		4	
	240			1		2	3	4		5	6	7
	320				2		4		6		8	
	400						5				10	
	480		1	2	3	4	6	8	9	10	12	14
	560						7				14	
	640				4		8		12		16	
	720			3		6	9	12		15	18	21
	800				5		10		15		20	
	960	1	2	4	6	8	12	16	18	20	24	28

TABLE 12

CLIPPER CORRELATOR REQUIREMENTS

Functions that are invarient as processors are added

	Boards	Cost
Limiter and Gate	4	$ 400
Shift Register	3	1,000
Mixer	1	100
40 MHz Oscillator and Distribution Amplifier	---	850
9.6 MHz Oscillator and Distribution Amplifier	---	850
		$3,200

Functions that are duplicated as processors are added

	Boards	Cost
(2) Mixers	2	$ 200
Output Amplifier	1	100
Bandpass Filter	---	100
Envelope Detector	2	200
Low Pass Filter	1	100
Delay Line & Associated Circuitry	---	3,500
Cabinet, Power Supplies, Misc.		500
		$4,700

TABLE 13

BASIC CLIPPER CORRELATOR COST

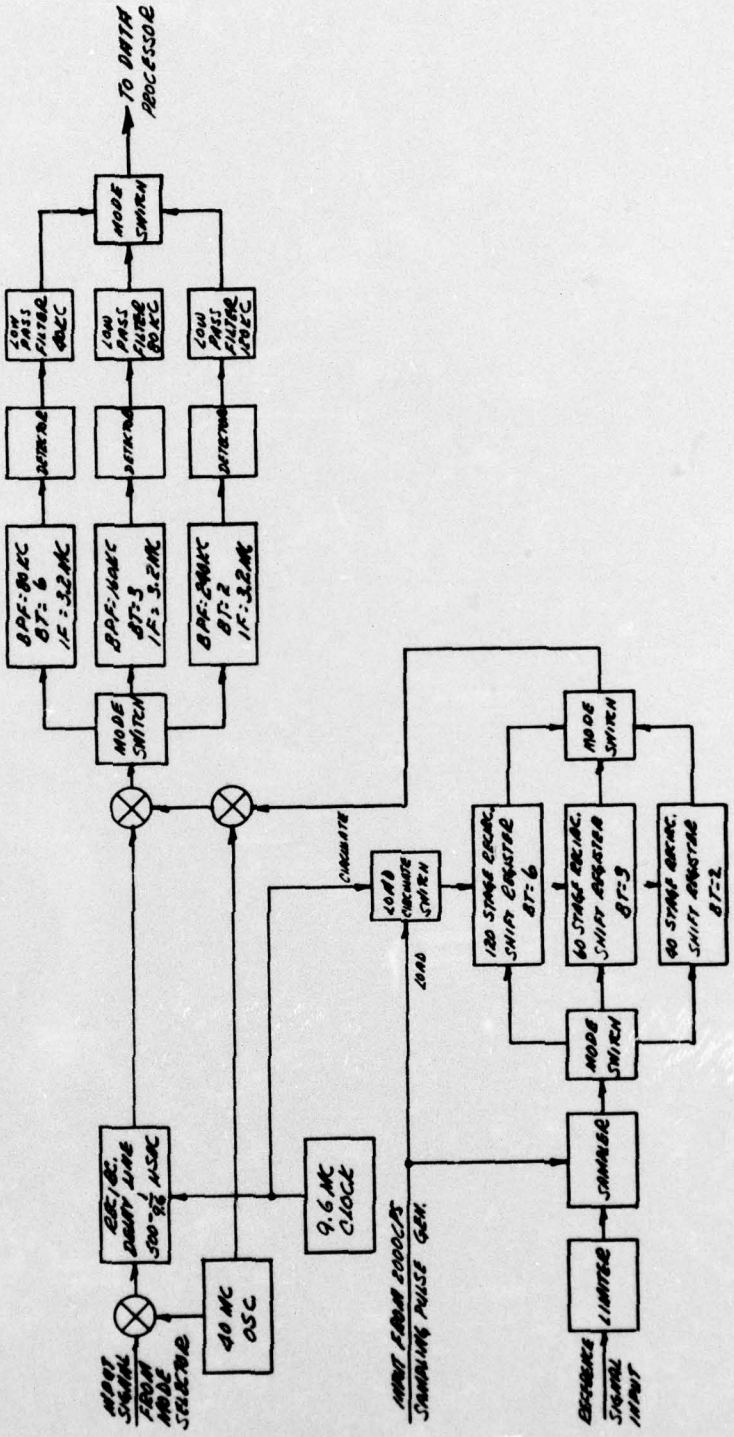

Figure 19. Clipper Correlator Block Diagram

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4. "Application of VICI to the Planar Array Sonar Signal Processing Problem", R. L. Brown, APDO, General Electric Company, Syracuse, New York, 12 July 1965.

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